Service Manual

Model 7014 DL7100/DL7200 Digital Oscilloscope

SM 701410-01E

YOKOGAWA
Yokogawa Electric Corporation

SM 701410-01E
3rd Edition

IMPORTANT NOTICE TO THE USER

This manual contains information for servicing YOKOGAWA's DL7100/DL7200 Series Digital Oscilloscopes. Check the serial number to confirm that this is the correct service manual for the instrument to be serviced. **Do not use the wrong manual**.

Before any maintenance and servicing, **read all safety precautions carefully**.

Only properly trained personnel may carry out maintenance and servicing described in this service manual.

Do not disassemble the instrument or its parts, unless otherwise clearly permitted by this service manual.

Do not replace any part or assembly, unless otherwise clearly permitted by this service manual.

In principle, Yokogawa Electric Corporation (YOKOGAWA) does not supply parts other than those listed in the customer maintenance parts list in this service manual (mainly modules and assemblies). Therefore if an assembly fails, the user should replace the whole assembly and not components within the assembly (see "**Note**"). If the user attempts to repair the instrument by replacing individual components within the assembly, YOKOGAWA assumes no responsibility for any consequences such as defects in instrument accuracy, functionality, reliability, or user safety hazards.

YOKOGAWA does not offer more detailed maintenance and service information than that contained in this service manual.

All reasonable efforts have been made to assure the accuracy of the content of this service manual. However, there may still be errors such as clerical errors or omissions. YOKOGAWA assumes no responsibility of any kind concerning the accuracy or contents of this service manual, nor for the consequences of any errors.

Disk No. SM12
3rd Edition : March 2002 (YK)

NOTE YOKOGAWA instruments have been designed in a way that the replacement of electronic parts can be done on an assembly (module) basis by the user. YOKOGAWA instruments have also been designed in a way that troubleshooting and replacement of any faulty assembly can be done easily and quickly. Therefore, YOKOGAWA strongly recommends replacing the entire assembly over replacing parts or components within the assembly. The reasons are as follows:

- The instruments use high-performance microprocessors, large scale CMOS gate arrays, and surface-mount components to provide state-of-the-art performance and functions.
- Repair of components can only be performed by specially trained and qualified maintenance personnel with special highly-accurate tools, including costly ones.
- When taking the service life and cost of the instruments into consideration, the replacement of assemblies offers the user the possibility to use YOKOGAWA instruments more effectively and economically with a minimum in downtime.

INTRODUCTION

This manual contains information for servicing YOKOGAWA DL7100/DL7200 Series Digital Oscilloscopes.

NOTE This manual is the third edition, March 2002.

WARNING

This service manual is to be used by properly trained personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the safety precautions prior to performing any servicing.
Even if servicing is carried out according to this service manual, or by qualified personnel, YOKOGAWA assumes no responsibility for any result occurring from that servicing.

SAFETY PRECAUTIONS

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings given elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument.
[Yokogawa Electric Corporation] assumes no liability for the customer’s failure to comply with these requirements.

General definitions of safety symbols used on equipment and in manuals



Explanation: To avoid injury, death of personnel or damage to the instrument, the operator must refer to an explanation in the instruction manual.



This symbol represents a functional grounding terminal. Such terminals should not be used as a “protective grounding terminal”.

WARNING

A **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death of personnel.

CAUTION

A **CAUTION** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part of the product.

WARNING

Power Supply

Ensure the source voltage matches the voltage of the power supply before turning ON the power.

Power Cord and Plug

To prevent an electric shock or fire, be sure to use the power supply cord supplied by YOKOGAWA. The main power plug must be plugged in an outlet with a protective grounding terminal. Do not invalidate protection by using an extension cord without protective grounding.

Protective Grounding

The protective grounding terminal must be connected to ground to prevent an electric shock before turning ON the power.

Necessity of Protective Grounding

Never cut off the internal or external protective grounding wire or disconnect the wiring of the protective grounding terminal. Doing so poses a potential shock hazard.

Defects in Protective Grounding or Fuses

Do not operate the instrument if you suspect the protective grounding or a fuse might be defective.

Fuse

To prevent a fire, make sure to use fuses with the specified standard (current, voltage, type). Before replacing the fuses, turn OFF the power and disconnect the power source. Do not use a different fuse or short-circuit the fuse holder.

Do Not Operate Near Flammable Materials
Do not operate the instrument in the presence of flammable liquids or vapors. Operation of any electrical instrument in such an environment constitutes a safety hazard.

Do Not Remove Any Covers
Some areas inside the instrument carry high voltage. Do not remove any cover, especially if the power supply is connected. The cover should be removed by qualified personnel only.

External Connection
To ground safely, connect the protective grounding before connecting the instrument to a measurement or control unit.

HOW TO USE THIS MANUAL

This manual is meant to be used by qualified personnel only. Make sure to read the safety precautions at the beginning of this manual as well as the warnings and cautions contained in the chapters relevant to any servicing you may be carrying out.

This manual contains the following chapters:

1 GENERAL INFORMATION
Provides an introduction, and describes safety considerations.

2 PERFORMANCE TEST
Describes the tests for checking the performance of the instrument.

3 ADJUSTMENTS
Describes the adjustments which can be performed by users.

4 PRINCIPLES OF OPERATION
Provides function block diagrams and describes the principles of operation.

5 TROUBLESHOOTING
Describes procedures for troubleshooting and how to proceed in case parts need to be replaced.

6 SCHEMATIC DIAGRAM
Provides a system configuration diagram.

7 CUSTOMER MAINTENANCE PARTS LIST
Contains exploded views and a list of replaceable parts.

Specifications are not included in this manual; for specifications, refer to IM 701410-01E.

CONTENTS

Chapter 1 GENERAL INFORMATION

This chapter provides the general information.

1.1 Introduction

This manual describes servicing information on any YOKOGAWA DL7100/DL7200 Series Digital Oscilloscopes.
This chapter contains information required for using this manual and information that must be read before starting servicing of DL7100/DL7200 series instruments.

1.2 Safety Considerations

You must thoroughly read the safety precautions at the beginning of this manual. Also fully read the warnings and cautions contained in each chapter.

Chapter 2 PERFORMANCE TEST

Contents of This Chapter

2.1 Introduction

The aim of the test is to check the basic performance of the instrument. The order of the test procedures is just for convenience and does not have any significant meaning. Please use recommended equipment or their equivalents.

2.2 Test Environment

1) Operate the instrument under the following conditions.
- Ambient temperature: 23 ±2 °C
- Humidity: 55 ±10% RH
- Voltage of power supply: Specified voltage ±1%
- Frequency of power supply: Specified frequency ±1%

2) Warm up time
- More than 30 minutes after turning ON the instrument.
- Confirm that self-calibration is correctly executed after the 30 minute warm up.
  (Be sure to Pay attention to the warm up time of all equipment that will be used in the test.)

2.3 Equipment Required for Performance Test

Equipment	Qty	Mandatory Specifications	Recommended
Calibrator	1	Accuracy ±0.05% Output voltage –40 V to 40 V Output resolution 1 mV Output frequency range 0.1 MHz to 500 MHz	WAVETEK 9500
Programmable head	1		WAVETEK 9520

2.4 Self_Diagnosis

Equipment Required

None

Procedure

Follow the procedure described in section 14.3, “Self-Diagnosis Test (Self-Test)” of the instruction manual (IM 701410-01E) .

2.5 Vertical Axis DC Voltage Accuracy Test

Specifications

2 mV/div to 50 mV/div: ±(1.5% of 8 div.+0.2 mV)
100 mV/div to 500 mV/div: ±(1.5% of 8 div.+2 mV)
1 V/div to 10 V/div: ±(1.5% of 8 div.+20 mV)

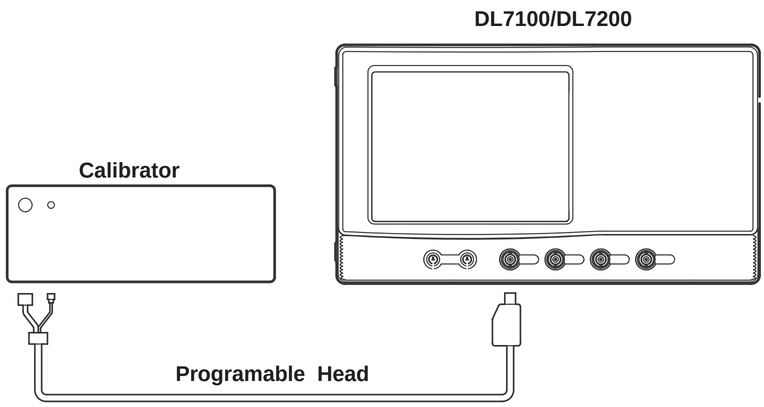
Permissible Range

Range	Tolerance
2 mV/div	±0.44 mV
5 mV/div	±0.8 mV
10 mV/div	±1.4 mV
20 mV/div	±2.6 mV
50 mV/div	±6.2 mV
100 mV/div	±14 mV
200 mV/div	±26 mV
500 mV/div	±62 mV
1 V/div	±140 mV
2 V/div	±260 mV
5 V/div	±620 mV
10 V/div	±1.22 V

Equipment Required

Equipment	Qty	Mandatory Specifications	Recommended
Calibrator	1	Accuracy ±0.05% Output voltage –40 V to 40 V Output resolution 1 mV	WAVETEK 9500
Programmable Head	1		WAVETEK 9520

Connection



Procedure

1) Turn on the power source of the DL7100/DL7200. After warm-up press the **MISC** key, followed by **Calibration** soft key, then press the **Cal Exec** soft key to calibrate the instrument.
   Next, press the **INITIALIZE** key, then press the **Initialize** soft key to initialize the settings.

2) Set the DL7100/DL7200 oscilloscope as shown below.

VERTICAL (for all channels)		
	Coupling	DC1 MΩ
	V/div	According to the inspection item below
	Probe	1:1
HORIZONTAL		
	T/div	1 ms/div
TRIGGER		
	Mode	Auto
ACQ		
	Mode	Box Average
	Count	Infinite
DISPLAY		
	Format	Single
MEASURE		
	Mode	ON
	Item Set Up	▼ (Set to channel to be measured)
		Select Avg.
	Time Range 1	–5 div
	Time Range 2	+5 div

3) Input the following voltages from the voltage generator to the DL7100/DL7200 to be tested, read the indication on the DL7100/DL7200 (value of Avg), and compare the reading with the tolerance.

Measurement Range	Test input voltage	Tolerance
2 mV/div	–8, 0, +8 mV	±0.44 mV
5 mV/div	–20, 0, +20 mV	±0.8 mV
10 mV/div	–40, 0, +40 mV	±1.4 mV
20 mV/div	–80, 0, +80 mV	±2.6 mV
50 mV/div	–200, 0, +200 mV	±6.2 mV
100 mV/div	–400, 0, +400 mV	±14 mV
200 mV/div	–800, 0, +800 mV	±26 mV
500 mV/div	–2, 0, +2 V	±62 mV
1 V/div	–4, 0, +4 V	±140 mV
2 V/div	–8, 0, +8 V	±260 mV
5 V/div	–20, 0, +20 V	±620 mV
10 V/div	–40, 0, +40 V	±1.22 V

4) Test all channels in the same manner.

2.6 Frequency Response Test

Specifications

DC50 Ω (1 V/div to 10 mV/div)	DC to 500 MHz (–3 dB point)
DC50 Ω (2 mV/div and 5 mV/div)	DC to 400 MHz (–3 dB point)

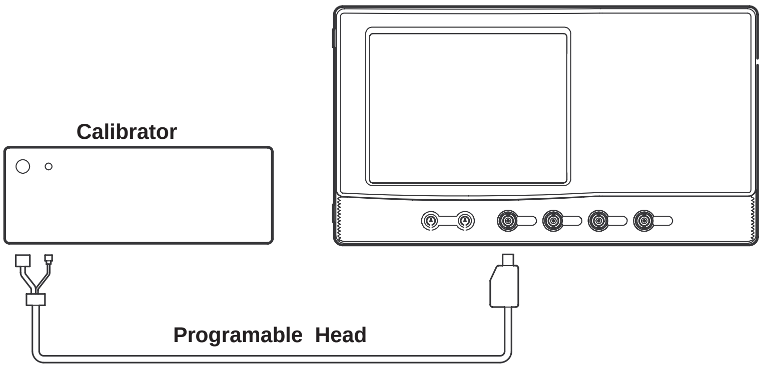
Permissible Range

Range	Input Amplitude (p-p)	Input Frequency	Permissible Range (Sdev)
1 V/div	5 V	500 MHz	1.26 V to 1.98 V
200 mV/div	1.2 V	500 MHz	301 mV to 476 mV
50 mV/div	0.3 V	500 MHz	75.1 mV to 119 mV
5 mV/div	30 mV	400 MHz	7.51 mV to 11.9 mV
2 mV/div	12 mV	400 MHz	3.01 mV to 4.76 mV

Equipment Required

Equipment	Qty	Mandatory Specifications	Recommended
Calibrator	1	Output voltage 0 V to 10 V Output resolution 1 mV Output frequency range 0.1 MHz to 500 MHz	WAVETEK 9500
Programmable Head	1		WAVETEK 9520

Connection



Procedure

1) Turn on the power source of the DL7100/DL7200. After warm-up press the **MISC** key, followed by **Calibration** soft key, then press the **Cal Exec** soft key to calibrate the instrument.
Next, press the **INITIALIZE** key, then press the **Initialize** soft key to initialize the settings.

2) Set the DL7100/DL7200 as shown below.

VERTICAL (for all channel)

Coupling	DC50 Ω
V/div	Set this according to following measurement conditions
Probe	1:1

HORIZONTAL

T/div	2 ns/div

TRIGGER	SIMPLE
Mode	Normal
SIMPLE	

Source (Channel to be tested)
ACQ
Mode Average
Count Infinite
Weight 4
Record Length 1 k
DISPLAY
Format Single
MEASURE
Mode ON
Item Set up ▼ (Set to channel to be tested)
Select Sdev
Time Range 1 –5.00 div
Time Range 2 +5.00 div

3) Input voltages as listed on the following table to the DL7100/DL7200 you are testing, and check if the automatically measured value of waveform parameters (Sdev) is within the permissible range.

Range	Input Amplitude (p-p)	Input Frequency	Permissible Range (Sdev)
1 V/div	5 V	500 MHz	1.26 V to 1.98 V
200 mV/div	1.2 V	500 MHz	301 mV to 476 mV
50 mV/div	0.3 V	500 MHz	75.1 mV to 119 mV
5 mV/div	30 mV	400 MHz	7.51 mV to 11.9 mV
2 mV/div	12 mV	400 MHz	3.01 mV to 4.76 mV

4) Test all channels in the same manner.

2.7 Time-Base Accuracy Test

Specifications

±0.005%

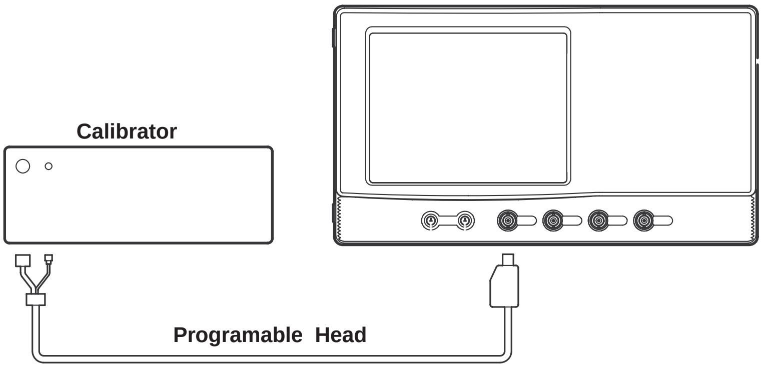
Permissible Range

Time Range	Input Frequency	Permissible Range
2 µs/div	500.2 MHz	200±25 kHz
5 µs/div	200.1 MHz	100±10 kHz

Equipment Required

Equipment	Qty	Mandatory Specifications	Recommended
Calibrator	1	300mVp-p, sine wave 200.1MHz and 500.2MHz	WAVETEK 9500
Programmable Head	1		WAVETEK 9520

Connection



Procedure

1) Turn on the power source of the DL7100/DL7200. After warm-up press the **MISC** key, followed by **Calibration** soft key, then press the **Cal Exec** soft key to calibrate the instrument.
   Next, press the **INITIALIZE** key, then press the **Initialize** soft key to initialize the settings.

2) Set the DL7100/DL7200 as shown below.

VERTICAL	
CH1	
V/div	50 mV/div
Coupling	DC50 Ω
Probe	1:1
HORIZONTAL	
T/div	According to the inspection item below
Display	
Format	Single
ACQ	
Record Length	10k
MEASURE	
Mode	ON
Item Set up	▼
CH1	Select Freq

3) Input a 300 mVp-p sine wave signal with the input frequency listed in the table below to the DL7100/DL7200 you are testing, and check if the automatically measured waveform parameters (Freq) are within the permissible range.

Time Range	Input Frequency	Permissible Range (Freq)
2 µs/div	500.2 MHz	200±25 kHz
5 µs/div	200.1 MHz	100±10 kHz

2.8 Trigger Sensitivity Test

Specifications

DC to 500 MHz: 1 divp-p on the screen

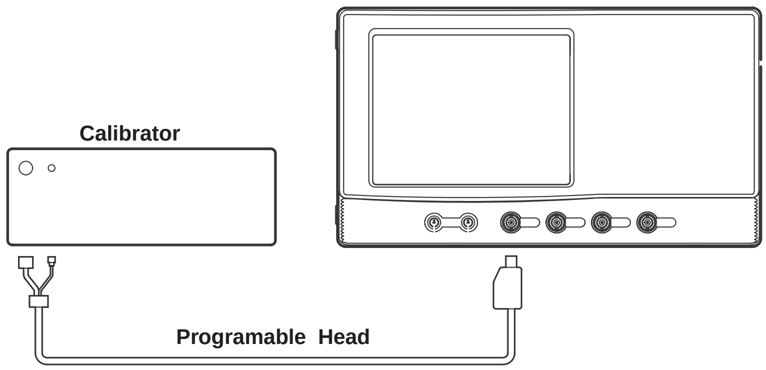
Permissible Range

500 mV/div 500 MHz 1 divp-p on the screen

Equipment Required

Equipment	Qty	Mandatory Specifications	Recommended
Calibrator	1	500 mVp-p, 500 MHz, sine wave	WAVETEK 9500
Programmable Head	1		WAVETEK 9520

Connection



Procedure

1) Turn on the power source of the DL7100/DL7200. After warm-up press the **MISC** key, followed by **Calibration** soft key, then press the **Cal Exec** soft key to calibrate the instrument.
Next, press the **INITIALIZE** key, then press the **Initialize** soft key to initialize the settings.

2) Set the DL7100/DL7200 as shown below.
VERTICAL (for all channels)
  V/div 500 mV/div
  Coupling DC50 Ω
  Probe 1:1
HORIZONTAL
  T/div 1ns/div
TRIGGER
  Mode Normal
  ENHANCED
    Type Pattern
    Set Pattern ▼
      Clock CH (Set to channel to be measured)
      Slope ↑ (channel to be measured)
      X (the other channel)

Condition	True
Level / Coupling	▼
Level	0 mV
Coupling	DC
DISPLAY	
Format	Single
ACQ	
Record Length	1 k
Mode	Average
Count	Infinite
Weight	4

3) Input a sine wave signal of 500 mVp-p 500 MHz to the DL7100/DL7200, and confirm that the waveform stabilizes.

NOTE If the trigger is not activated, adjust the trigger lever within ±250 mV until the trigger is activated.

4) Test all channels in the same manner.

2.9 Trigger Accuracy Test

Specifications

±(1 div.+10% of the trigger level)

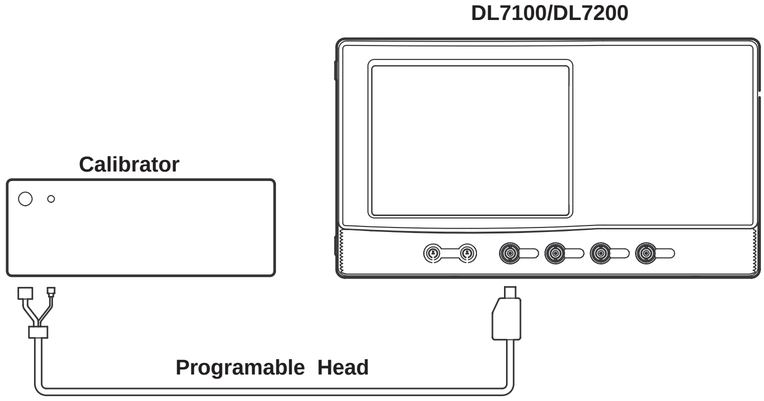
Permissible Range (when 200 mV/div)

Trigger level	Offset	Permissible Range
600 mV	600 mV	–260 mV ≤ (Vin + Vout) / 2 ≤ 260 mV
–600 mV	–600 mV	–260 mV ≤ (Vin + Vout) / 2 ≤ 260 mV

Equipment Required

Equipment	Qty	Mandatory Specifications	Recommended
Calibrator	1	400mVp-p, 2kHz, sine wave	WAVETEK 9500
Programmable head	1		WAVETEK 9520

Connection



Procedure

1) Turn on the power source of the DL7100/DL7200. After warm-up press the **MISC** key, followed by **Calibration** soft key, then press the **Cal Exec** soft key to calibrate the instrument.
Next, press the **INITIALIZE** key, then press the **Initialize** soft key to initialize the settings.

2) Set the DL7100/DL7200 oscilloscope as follows.
VERTICAL (for all channels)
    V/div 200 mV/div
    Probe 1:1
    Band Width 20 MHz
    Offset –600 mV, 600 mV
HORIZONTAL
    T/div 100 µs/div
TRIGGER
  ENHANCED
    Type OR
    Window ON
    Set Pattern ▼
        IN, OUT (channel to be measured)
        – (the other channel)
    Level / Coupling ▼
      Center –600 mV, 600 mV
      Width 1.2 V
  DISPLAY
    Format Single
  CURSOR
    Type Marker
    Position 0.0 div

3) Input a sine wave signal of 400 mVp-p, 2 kHz to the DL7100/DL7200 oscilloscope, and use cursors to read the voltage of the waveform at the trigger position. Set **Vin** for Polarity IN, **Vout** for Polarity out, and check if (Vin+Vout)/2 is within the permissible range.

Trigger level	Offset	Permissible Range
600 mV	600 mV	–260 mV ≤ (Vin + Vout) / 2 ≤ 260mV
–600 mV	–600 mV	–260 mV ≤ (Vin + Vout) / 2 ≤ 260mV

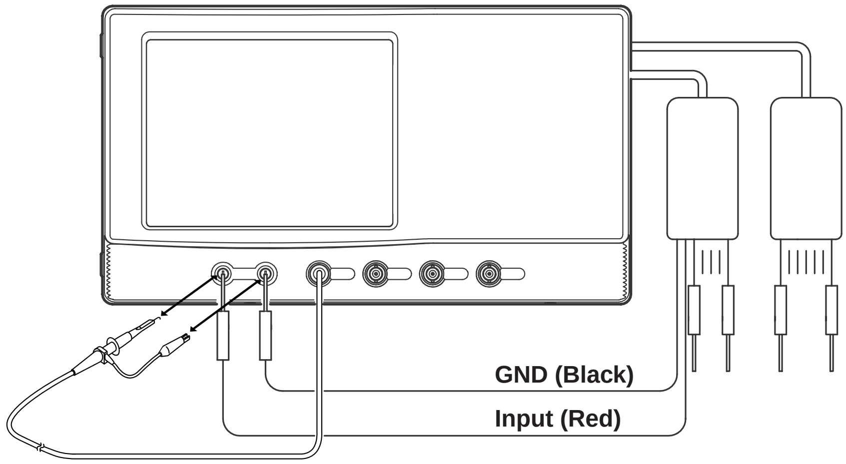
4) Test all channels in the same manner.

2.10 Logic Input Function Test

Equipment Required

Equipment	Qty	Mandatory Specifications	Recommended
Probe	1	400 MHz frequency range	Yokogawa 700988
Logic Probe	2	8 bit	Yokogawa 700985

Connection



Procedure

1) Turn on the power of the DL7100/DL7200 and press the **INITIALIZE** key, then press the **Initialize** soft key to initialize the settings.
2) Press the **AUTO SETUP** key and select the **Auto Setup** soft key.
3) Press the **LOGIC** key, press the **Mode** function key, then select the **ON**.
4) Press the **Select** function key and select the **Pod A** soft key.
5) Press the **Level** function key, select the **User** soft key, and turn the jog shuttle to **0.5V**.
6) Set POD B in the same manner as POD A.
7) Press the **ENHANCED** key, press the **Type** function key, and select the **Logic** soft key.
8) Press the **Set Pattern** function key, set the Clock CH to **None** and set **Condition** to **Enter**.
9) Set the 1st bit status of POD A to **H**. The other bits and the bits of the other POD are set to **X**.
10) Connect the 1st bit probe of POD A to the PROBE COMPENSATION output terminal.
11) Check whether the trigger activated correctly. If the logic input signal is displayed, check the waveform on the screen.
12) Change the connection of the probe and test the other bits in the same manner.
13) Change the connection of POD B and test POD B in the same manner.

Chapter 3 ADJUSTMENTS

Contents of This Chapter

3.1 Introduction

The main unit cover must be removed before adjusting the DL7100/DL7200 read the warning and caution below before doing so.

WARNING

Circuit patterns of the printed circuit board are exposed. Be careful when handling so that hands or fingers are not injured by the protruding pins.

CAUTION

- Circuit patterns of the printed circuit board are exposed. If these patterns touch other metallic materials, electrical shorting will occur, causing the circuit to be damaged or burnt.
- It is sometimes necessary to turn the DL7100/DL7200 upside down for adjustment. Do not drop, or allow the instrument to fall over.
- When feeding power with the DL7100/DL7200's cover open, apply a flow of air to the AD board.

3.2 Test Environment

1) Operate the instrument under the following conditions.

- Ambient temperature: 23 ±2 ˚C
- Humidity: 55 ±10 % RH
- Voltage of power supply: Specified voltage ±1 %
- Frequency of power supply: Specified frequency ±1 %

2) Warm up time

- More than 30 minutes after tuning ON the instrument.
- Confirm that self calibration is correctly executed after a 30 minute warm up.
  (Be sure to pay attention to the warm up time of all equipment that will be used in the test.)

3.3 Equipment Required

Table 3.1 Equipment required

Equipment	Critical Specification	Recommended
Calibrator Programmable Head	DC Output Level : 1 V Accuracy : < 0.02% Square wave Frequency : 10 kHz Output Level : > 60 Vp-p	WAVETEK 9500 WAVETEK 9520

NOTE The values shown in the specification column are those set in this service manual. These values do not indicate the performances of the recommended equipment and tools. Therefore, non-designated equipment and tools which satisfy the specifications may be permitted for use.

3.4 DC Gain Adjustment on the AD board

Procedure

1) Remove the main unit cover.
2) Allow the unit to warm up for 10 minutes or more.
3) Connect each instrument as shown in Figure 3.1 Connection method.

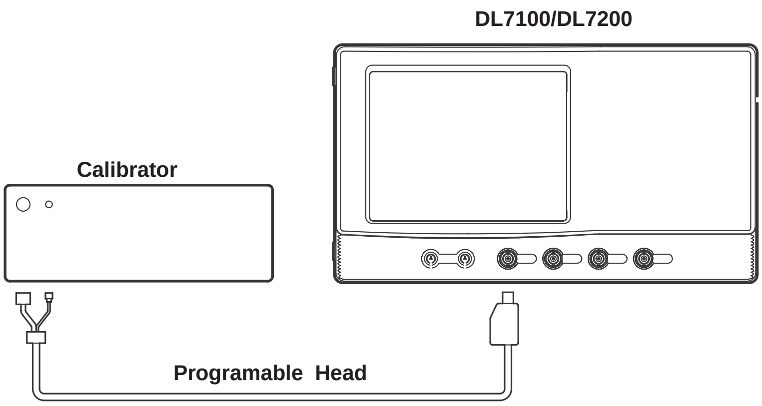


Figure 3.1 Connection Method

4) Press the **INITIALIZE** key and select the **Initialize** soft key to execute initialization.
5) Press the **MISC** key and select the **Calibration** soft key.
6) Press the **Cal Exec** soft key to perform calibration.

7) Set up the DL7100/DL7200 and calibrator as follows.

DL7100/DL7200	VERTICAL (for all channels)		
		V/div	2 mV/div
		Position	0 div
		Probe	1:1
		Offset	+1.000 V
		Bandwidth	20 MHz
	HORIZONTAL		
		T/div	1 ms/div
	TRIGGER		
		Mode	Auto
	ACQ		
		Mode	Box Average
		Count	Infinite
	DISPLAY		
		Format	Single
	MEASURE		
		Mode	ON
		Item Set Up	▼(Set to channel to be measured) Select Avg.
		Time Range 1	-5 div
		Time Range 2	+5 div
Calibrator	DC Output Level		+1.0000 V

8) Adjust the variable resistor (refer to table 3.2, “ Adjustment Point” and figure 3.2,3.3, “Adjustment Point Location Diagram”) corresponding to each channel so that the DC wave form fits within 1 V±1 mV as shown in figure 3.4, “Observed Waveform.”
9) Perform the adjustment of 7) for all channels.

Table 3.2 Adjustment Point

Channel	Adjustment Point
ch1	R707
ch2	R714
ch3	R721
ch4	R728

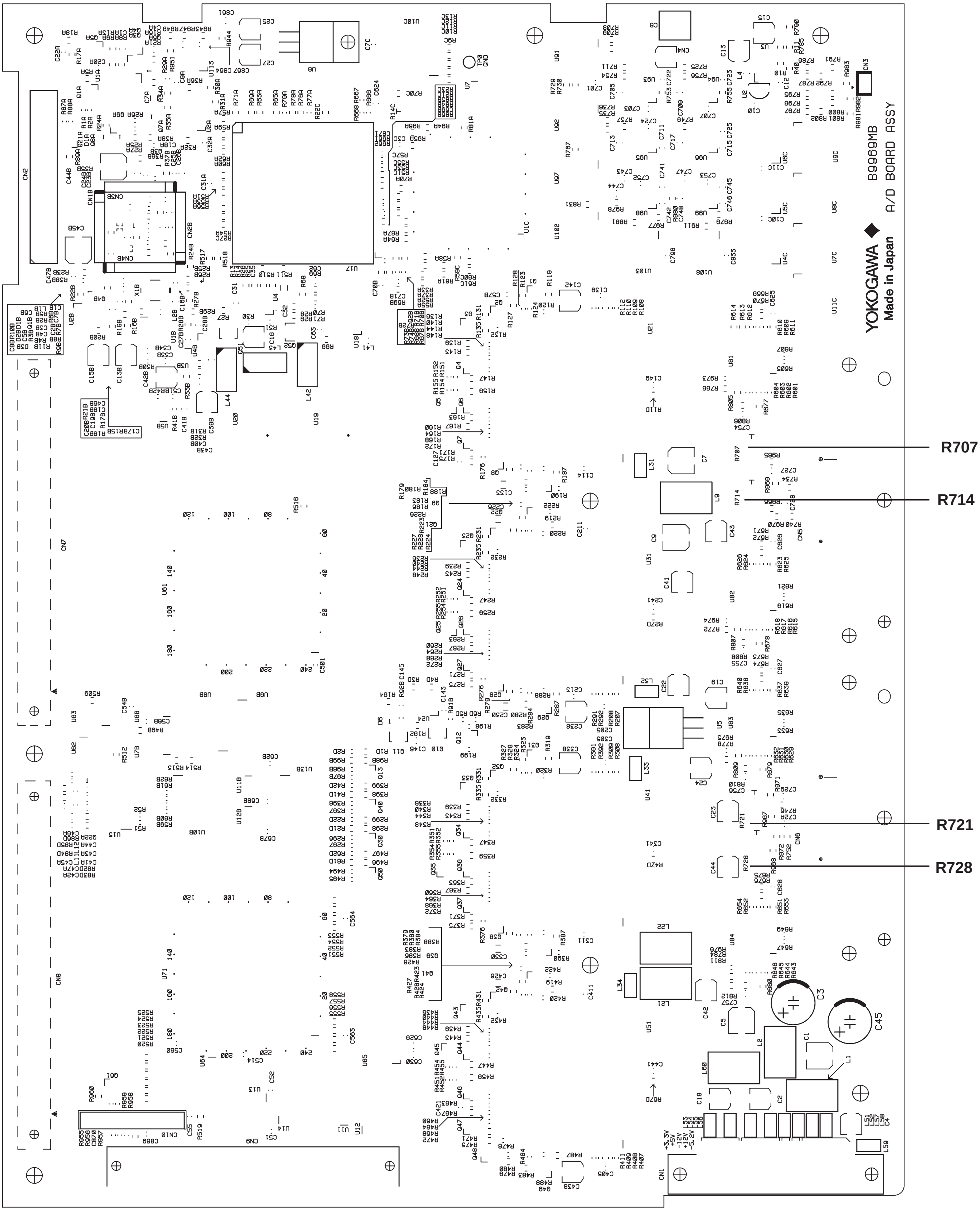


Figure 3.2 Adjustment Point Location Diagram (DL7100)

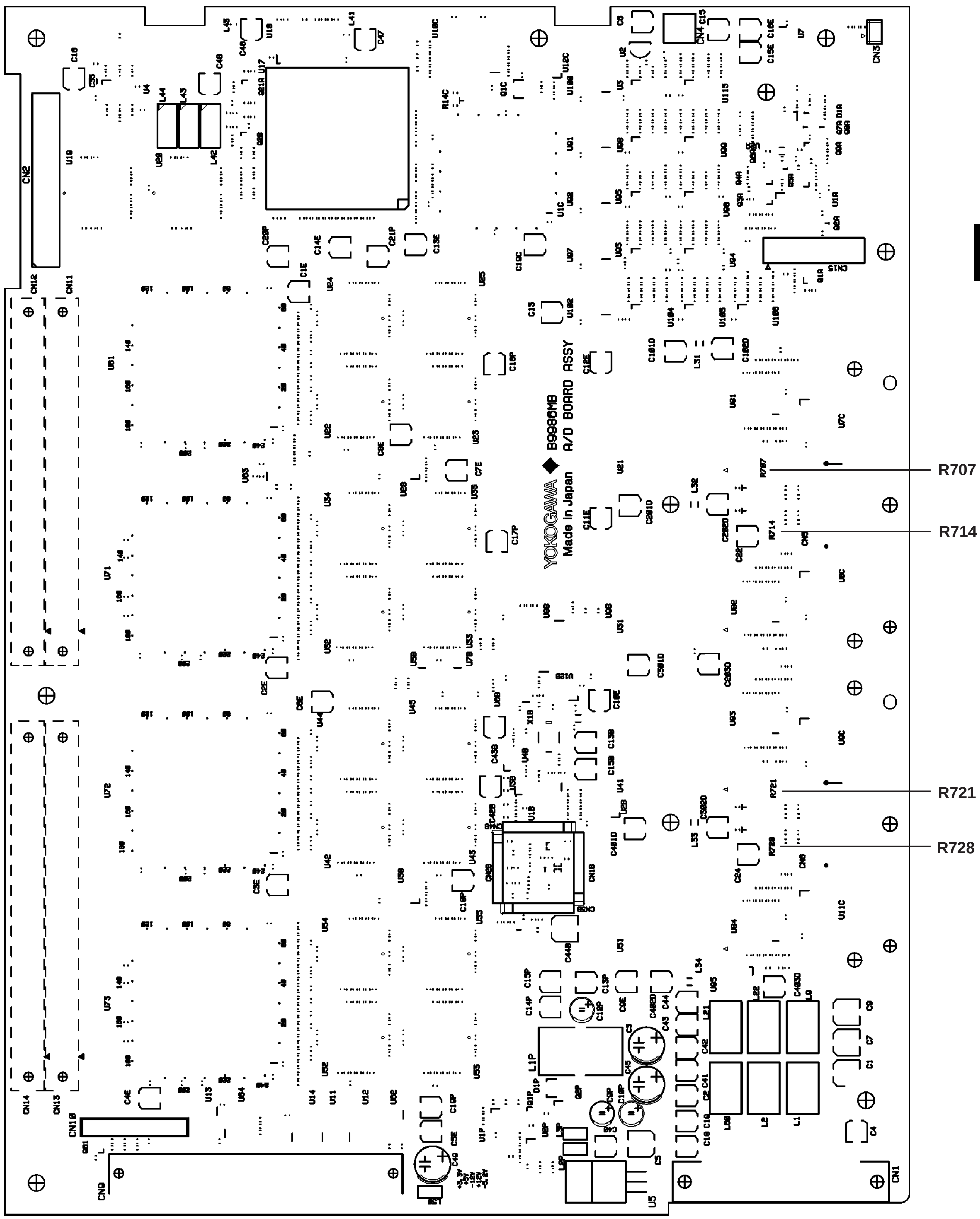


Figure 3.3 Adjustment Point Location Diagram (DL7200)

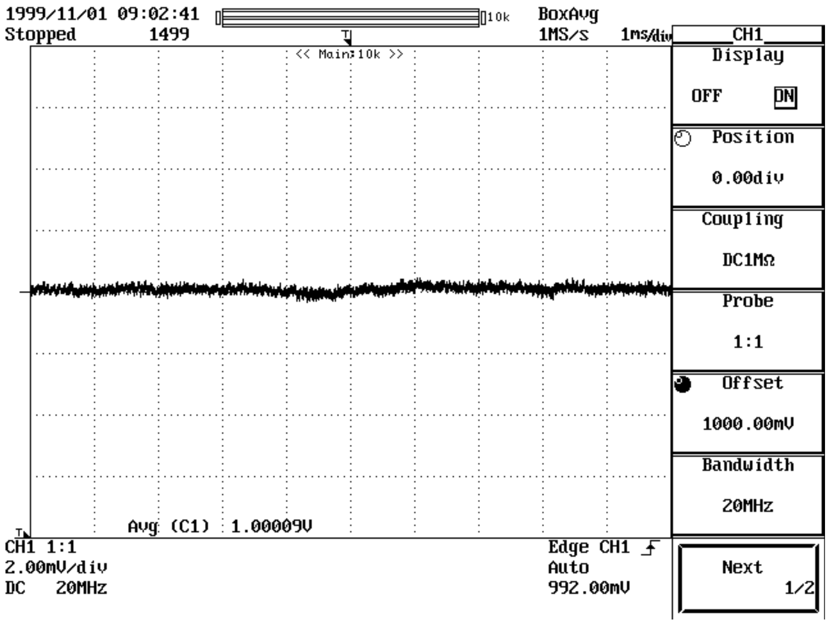


Figure 3.4 Observed Waveform

3.5 Flatness Adjustment on the Analog Board

NOTE Before performing this flatness adjustment, the DC gain adjustment on the AD board must have been completed.

Procedure

1) Remove the main unit cover.
2) Turn on the power and allow the unit to warm up for 10 minuets or more.
3) Connect each instrument as shown in figure 3.5, “Connection Method.”

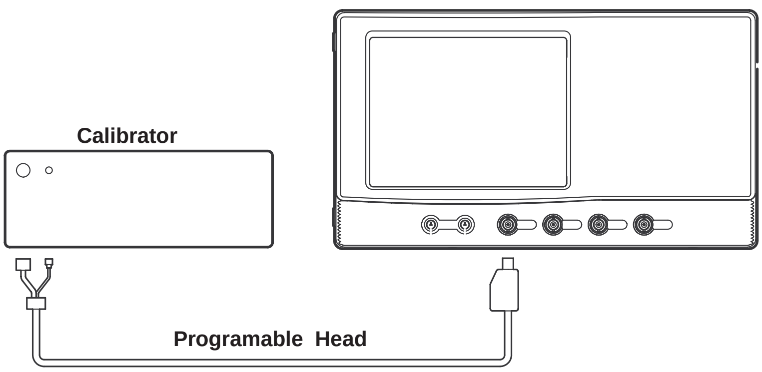


Figure 3.5 Connection Method

4) Press the **INITIALIZE** key and select the **Initialize** soft key to execute initialization.
5) Press the **MISC** key and select the **Calibration** soft key.
6) Select the **Cal Exec** soft key to perform calibration.

7) For adjustment of the /10 range, set up the DL7100/DL7200 oscilloscope and calibrator as follows.

DL7100/DL7200	VERTICAL (for all channels)		
		V/div	100 mV/div
		Position	0 div
		Probe	1:1
	HORIZONTAL		
		T/div	10 μs/div
	TRIGGER		
		Mode	Auto
	ACQ		
		Mode	Box Average
		Count	Infinite
	DISPLAY		
		Format	Single
Calibrator	Wave Form		Square wave
	Frequency		10 kHz
	Amplitude		600 mVp-p

8) Adjust the variable capacitors CV101 and CV201, (refer to figure 3.6, "Adjustment Point Location Diagram") so that the top of the waveform becomes flat as shown in figure 3.7, "Observed Waveform." The flatness of the waveform must be fitted within ±0.1 div.

9) For adjustment of the /100 range, set up the DL7100/DL7200 oscilloscope and calibrator as follows.

DL7100/DL7200	VERTICAL (for all channels)		
		V/div	1 V/div
		Position	0 div
		Probe	1:1
	HORIZONTAL		
		T/div	10 μs/div
	TRIGGER		
		Mode	Auto
	ACQ		
		Mode	Box Average
		Count	Infinite
	DISPLAY		
		Format	Single
Calibrator	Wave Form		Square wave
	Frequency		10 kHz
	Amplitude		6 Vp-p

10) Adjust the variable capacitors CV102 and CV202 (refer to figure 3.6, "Adjustment Point Location Diagram") so that the top of the waveform becomes flat as shown in figure 3.7, "Observed Waveform." The flatness of the waveform must be fitted within ±0.1 div.

11) For adjustment of the /200 range, set up the DL7100/DL7200 oscilloscope and calibrator as follows.

DL7100/DL7200	VERTICAL (for all channels)		
		V/div	10 V/div
		Position	0 div
		Probe	1:1
	HORIZONTAL		
		T/div	10 µs/div
	TRIGGER		
		Mode	Auto
	ACQ		
		Mode	Box Average
		Count	Infinite
	DISPLAY		
		Format	Single
Calibrator	Wave Form		Square wave
	Frequency		10 kHz
	Amplitude		60 Vp-p

12) Adjust the variable capacitors CV103 and CV203 (refer to figure 3.6, “Adjustment Point Location Diagram”) so that the top of the waveform becomes flat as shown in figure 3.7, “Observed Waveform.” The flatness of the waveform must be come within ±0.1 div.

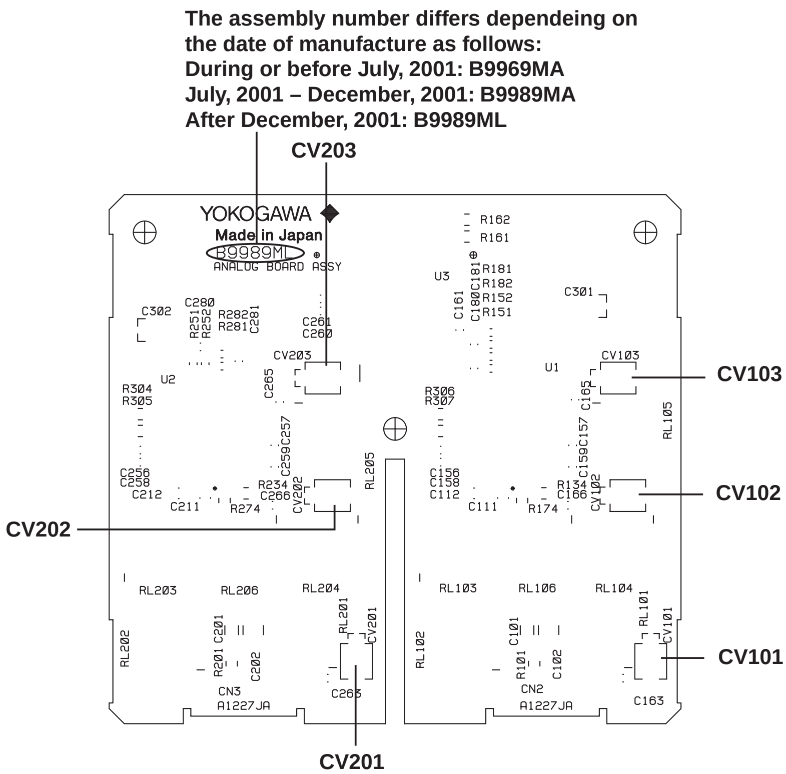


Figure 3.6 Adjustment Point Location Diagram

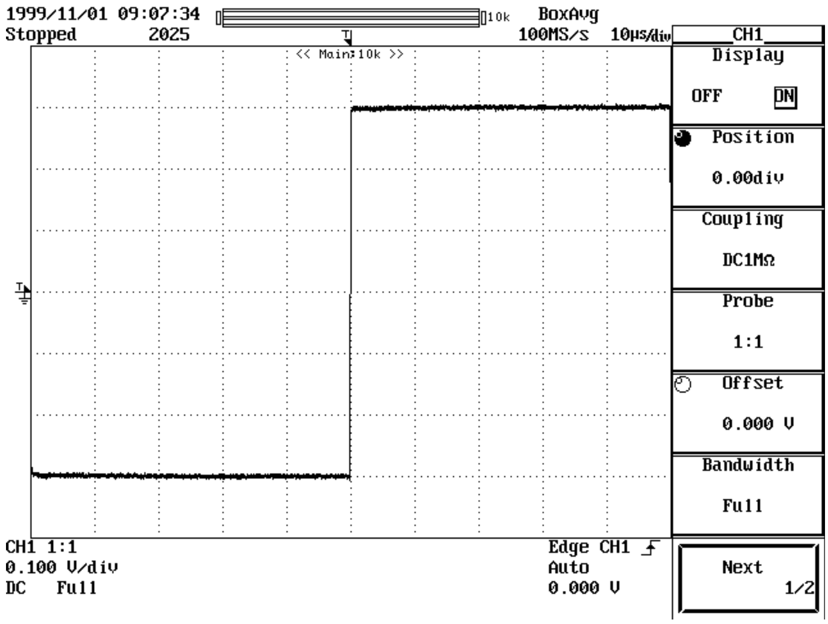


Figure 3.7 Observed Waveform

3

ADJUSTMENTS

Chapter 4 PRINCIPLES OF OPERATION

Contents of This Chapter

4.1 Introduction

The block diagrams of the DL7100 are shown in figure 4.1 and figure 4.2.
The block diagrams of the DL7200 are shown in figure 4.3 and figure 4.4.
Figure 4.1 and figure 4.3 are block diagrams of the circuit from the analog input to the data acquisition circuit including the attenuator, one-chip amplifier, analog multiplexer, A/D converter, trigger comparator, trigger circuit, and the ring buffer memory and its controller.
Figure 4.2 and figure 4.4 are block diagrams of (1) the data processing section which processes the acquired data and displays the waveform, (2) the CPU, and (3) the peripheral circuitry. In addition, figure 4.2 and figure 4.4 include a block diagram of the logic input circuit.

4.2 Function of Each Assembly

This section describes the ATT board assembly and AFC board assembly.

(1) Analog Board Assembly

The analog board assembly has a coupling switch for AC/DC, 1 MΩ/50 Ω, and GND/ Measure and a switch circuit for the attenuator (1:1/10:1/100:1/200:1). Relays are used to make the switch. In addition, a one-chip amplifier IC and an analog multiplexer IC are onboard.

The one-chip amplifier IC has a gain switch circuit, a low-pass filter circuit (external capacitor), a trigger coupling circuit (external capacitor), and a trigger bandwidth limiting circuit (external capacitor). In addition, the input offset voltage and the trigger level are varied using an external DC voltage input. The frequency bandwidth of the IC is approximately 600 MHz.

As indicated in figure 4.1, the vertical sensitivity from 10 V/div to 2 mV/div is achieved by switching the gain on the attenuator and the one-chip amplifier IC.

The analog multiplexer IC is used to achieve the interleave operation.
During the interleave operation, the input signal of CH1 (CH3) is supplied to the A/D converter of CH2 (CH4).
The frequency bandwidth of the IC is approximately 2 GHz.

The above-mentioned control signal, offset, and DC voltage for the trigger level are supplied by the analog front-end controller (AFC) on the AD board assembly.

Table 4.1 Setting Range and Amplifying Level

Setting Range	Attenuator Division Ratio	Amplifying Rate
2 mV/div	1/1	x25
5 mV/div	1/1	x10
10 mV/div	1/1	x5
20 mV/div	1/1	x2.5
50 mV/div	1/1	x1
100 mV/div	1/10	x5
200 mV/div	1/10	x2.5
500 mV/div	1/10	x1
1 V/div	1/100	x5
2 V/div	1/100	x2.5
5 V/div	1/100	x1
10 V/div	1/200	x1

The setting range here is for the 1:1 probe setting.

(2) AD Board Assembly

The AD board assembly has the time base, trigger, A/D converter, ring buffer controller (RBC), and analog control circuits onboard.

The time base is of a PLL configuration. 1 GHz and 800 MHz can be switched. On the DL7100, the frequency of the clock is converted to 500 MHz or 400 MHz using high-speed ECL logic and distributed to each channel. When in interleave mode, the clock for CH2 and CH4 is delayed by 1 ns with respect to the clock for CH1 and CH3, respectively. On the DL7200, the 1-GHz or 800-MHz clock is distributed to each channel without any frequency conversion. When in interleave mode, the clock for CH2 and CH4 is delayed by 500 ps with respect to the clock for CH1 and CH3, respectively. For making minute time measurements of phase difference between the trigger and sampling clock (needed during repetitive sampling mode, for example), the T-V converter (TVC) is used.

The trigger section consists of a comparator, fast trigger logic (FTL), and pulse width detector (PWD). It also has a TV trigger circuit used only on CH1. The comparator has a window comparator function that allows window triggering. The window width is controlled by an external DC voltage input. The frequency bandwidth of the comparator IC is 1 GHz.

On the DL7100, the A/D converter operates at 500 MHz only when the sampling rate is 500 MS/s or when in 1 GS/s interleave mode. In all other cases, the A/D converter operates at 400 MHz. Sampling rates of 200 MS/s or lower are attained by extracting a portion of the data sampled at 400 MHz using the RBC. On the DL7200, the A/D converter operates at 1 GHz only when the sampling rate is 500 MS/s or 1 GS/s or when in 2 GS/s interleave mode. In all other cases, the A/D converter operates at 800 MHz. A sampling rate of 500 MS/s is attained by extracting a portion of the data sampled at 1 GHz using the RBC. Sampling rates of 200 MS/s or lower are attained by extracting a portion of the data sampled at 800 MHz using the RBC.

The RBC performs primary processing such as the above-mentioned data extraction of sampled data, envelope, and box averaging, then stores the data in the ring buffer memory. The written data are transferred to the acquisition memory interface (AMI) on the CPU board assembly according to the trigger address.

The analog control circuit consists of an analog front-end controller (AFC), a PWM D/A converter, and a serial/parallel converter. This circuit controls the analog section of the analog board assembly and the AD board assembly.

(3) Ring Bufer Memory Board Assembly

The ring buffer memory board assembly consists of a fast bus buffer (FBB) and ring buffer memory (fast SRAM).
The 701410 and 701420 use a 1-Mbit SRAM and a 4-Mbit SRAM, respectively.
The 701430 and 701440 have twice the amount of SRAM that the 701410 and 701420 have, respectively.

(4) CPU Board Assembly

The CPU board assembly consists of the secondary data processing section, a display section (for displaying waveforms and other information), the CPU, and its peripheral circuits.

The secondary data processing section consists of an acquisition memory interface (AMI), work memory (PBSRAM), and the acquisition memory on the ACQ memory board assembly. The AMI processes the data (averaging, for example) that are transferred from the RBC on the AD board assembly and stores the result in the acquisition memory. Then, the AMI converts the stored data to display data by performing additional processing such as compression and interpolation. The resultant data are transferred to the graphic control process (GCP) according to the display update interval. The AMI also has the computation function (addition, subtraction, multiplication, division, differentiation, integration, etc.) and auxiliary functions such as automated measurement of waveform parameters.

The display section consists of a GCP, graphic memory (synchronous GRAM), character memory (fast SRAM), and VGA VIDEO OUT circuits. The GCP writes the waveform data that are transferred from the AMI (includes the AMI on the logic board assembly) to the graphic memory. It synthesizes the contents of the graphic memory and the character memory and displays them on the TFT color LCD. The GCP also controls the built-in printer.

The CPU is Hitachi's HD6417709A operating at 66 MHz. The CPU peripheral circuits include the main memory (synchronous DRAM), flash memory, backup memory, a GPIB controller, a SCSI controller, an FDD controller, a Centronics interface, and an RS-232 interface. The CPU I/O interface (CIO) controls a part of these peripheral circuits.

(5) ACQ Memory Board Assembly

The ACQ memory board assembly has an acquisition memory (synchronous DRAM) onboard. It is controlled by the acquisition memory interface (AMI) on the CPU board assembly. The acquisition memory uses a 64-Mbit synchronous DRAM. The 701430 and 701440 uses twice the amount of 64-Mbit synchronous RAMs as the 701410 and 701420.

(6) Logic Board Assembly (Option)

The logic board assembly consists of an interface section of the logic probe, a data acquisition section, and a logic trigger circuit. The interface section supplies power to the logic probe and provides a buffer for the logic input. Similar to the analog input section, the data acquisition section has an RBC, a ring buffer memory, an AMI, acquisition memory, and a work memory. For the ring buffer memory, a 1-Mbit SRAM is used for option /N1, /N3 and a 4-Mbit SRAM is used for option /N2, /N4.
Option /N3 and option /N4 use twice the amount of SRAM as option /N1 and option /N2, respectively.

(7) Rear Board Assembly

The rear board assembly provides EXT CLOCK IN/EXT TRIG IN/TRIG GATE IN and TRIG OUT.

This board supplies the power source (+12V, -12V) for the active probes.

(8) Key Board Assembly

Key switches, LEDs, the rotary encoder, and the jog shuttle are installed on the key board assembly.

(9) Line Trigger Board Assembly

The AC Line input from the inlet is supplied to the power supply unit across the switch on the line trigger board assembly.

This assembly also contains the line trigger circuit.

(10) Power Board Assembly

The power board assembly distributes the DC voltage output from the power supply unit to the AD board assembly, ring buffer memory board assembly, and CPU board assembly.

(11) Bus Board Assembly

The CPU board assembly and the AD board assembly exchange signals via the bus board assembly.

(12) LCD Board Assembly

The LCD board assembly converts the connector of the LCD signal cable.

(13) LCD Assembly

8.4-inch color TFT LC display

Full display resolution: 640 x 480

Waveform display resolution: 500 x 384

(14) Printer Assembly (Option)

The printer is of a thermal sensitivity type that prints 8 dots per mm and 832 dots per line. A hardcopy of the display is printed in approximately 12 seconds.

(15) FDD Assembly

The FDD assembly supports 3.5-inch floppy disks with the formats of 640 KB, 720 KB, 1.2 MB, and 1.44 MB.

(16) Ethernet + PC Card Interface Board Assembly (option)

Option /C9 consists of a PC card interface section. Option /C10 consists of a PC card interface section and an Ethernet interface section. The PC card interface section has a PC card slot and a PC card controller. The Ethernet interface section has an Ethernet connector and a LAN (local area network) controller. These interfaces are controlled by the CPU and CPU I/O interface (CIO) that are on the CPU board assembly.

(17) OPT TRIG Board Assembly (option)

Option /F7 consists of a CANBus Trigger section. The OPT TRIG Board Assembly provide CANBus Trigger signal.

4.3 Function of Each ASIC

The following items describe the IC and the gate array function used in each assembly.

(1) Analog Front-End Controller (AFC)

The AFC is a Bi-CMOS gate array. Its main functions are controlling the analog front-end circuit and assisting the trigger circuit. It has a PWM signal output circuit used for D/A conversion, a parallel port, a serial port, a trigger hold-off circuit, an auto trigger circuit, a TV trigger generator, a fast counter, and a slow counter, etc.

(2) Fast Trigger Logic (FTL)

The FTL is an ECL gate array. Its main functions include generation of trigger signals according to the trigger functions, trigger hold-off function, and the control of the time-to-voltage converter (TVC).

(3) Pulse Width Detector (PWD)

The PWD is an analog IC. Using an internally-startable oscillator and an external counter (AFC), it detects the pulse width for width triggering.

(4) Time-to-Voltage Converter (TVC)

This is the analog IC that measures the internal sampling clock and trigger time, and coverts time to voltage.

(5) Ring Buffer Memory Controller (RBC)

The RBC is a Bi-CMOS gate array. It performs primary processing of the data such as the extraction of the sampled data, envelope, and box averaging. It also provides functions for controlling the ring buffer memory and the interface to the acquisition memory interface (AMI).

(6) Fast Bus Buffer (FBB)

The FBB is a CMOS gate array. Its function is to provide a buffer for the data bus, address bus, and control signal between the ring buffer memory controller (RBC) and the ring buffer memory.

(7) Acquisition Memory Interface (AMI)

The AMI is a CMOS gate array. Its functions include interface to the ring buffer memory controller (RBC), interface to the graphic control processor (GCP), averaging, history control, waveform computation, and auxiliary functions for the automated measurement of waveform parameters.

(8) Graphic Control Processor (GCP)

The GCP is a CMOS gate array. Its functions include interface to the acquisition memory interface (AMI), graphic memory and character memory control, waveform drawing function (accumulated display, for example), built-in printer control, and display data generation for the LCD.

(9) CPU I/O Interface (CIO)

The CIO is a CMOS gate array. Its functions include interface to the CPU (HD6417709A) and the peripheral ICs, keyboard control, LED control, interrupt control, and DMA selection.

(10) CANBus Trigger Logic (CTL)

The CTL is Field Programmable Gate array. Its function is generation of CANBus trigger signal.

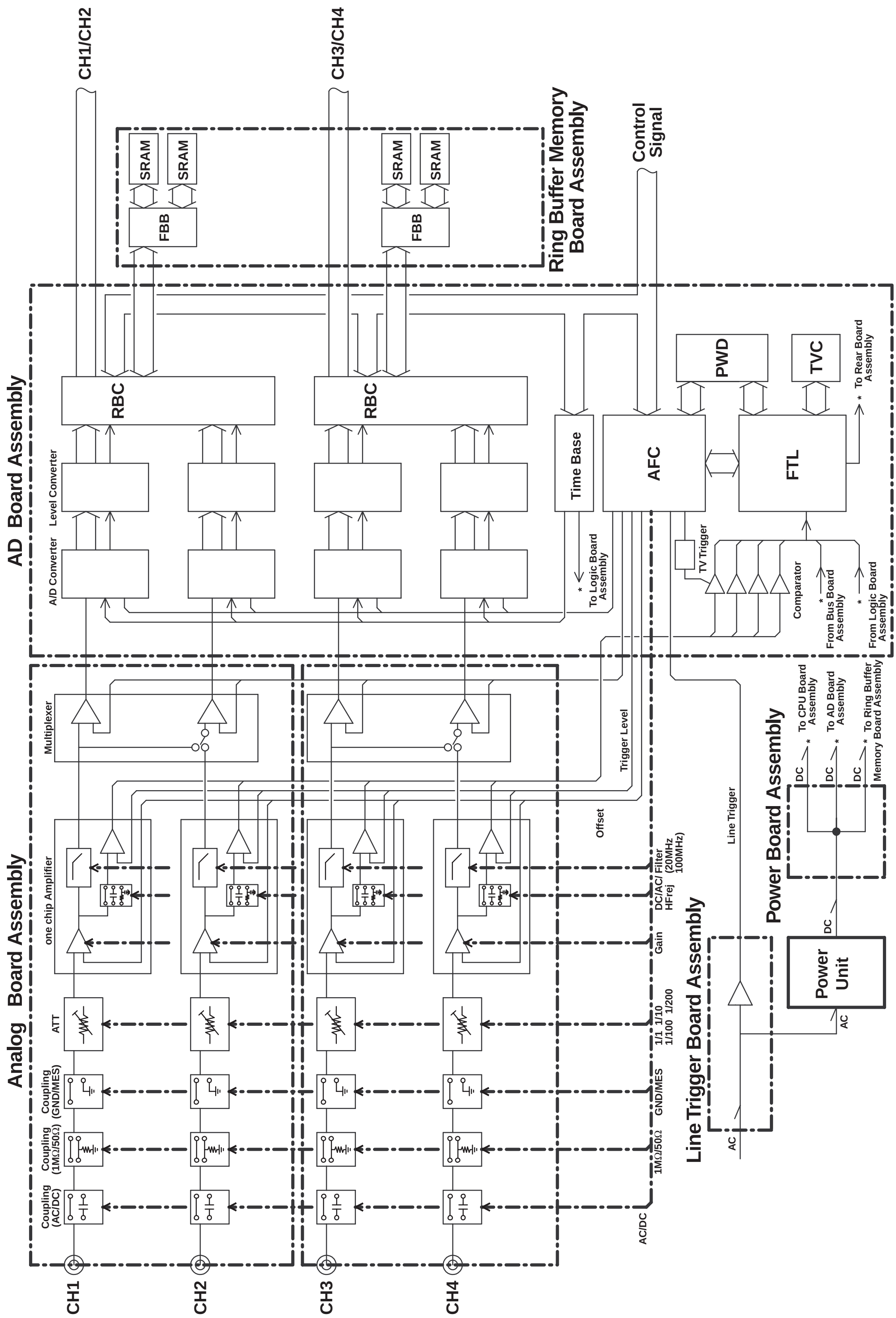


Figure 4.1 Block Diagram (Analog Section) of the DL7100

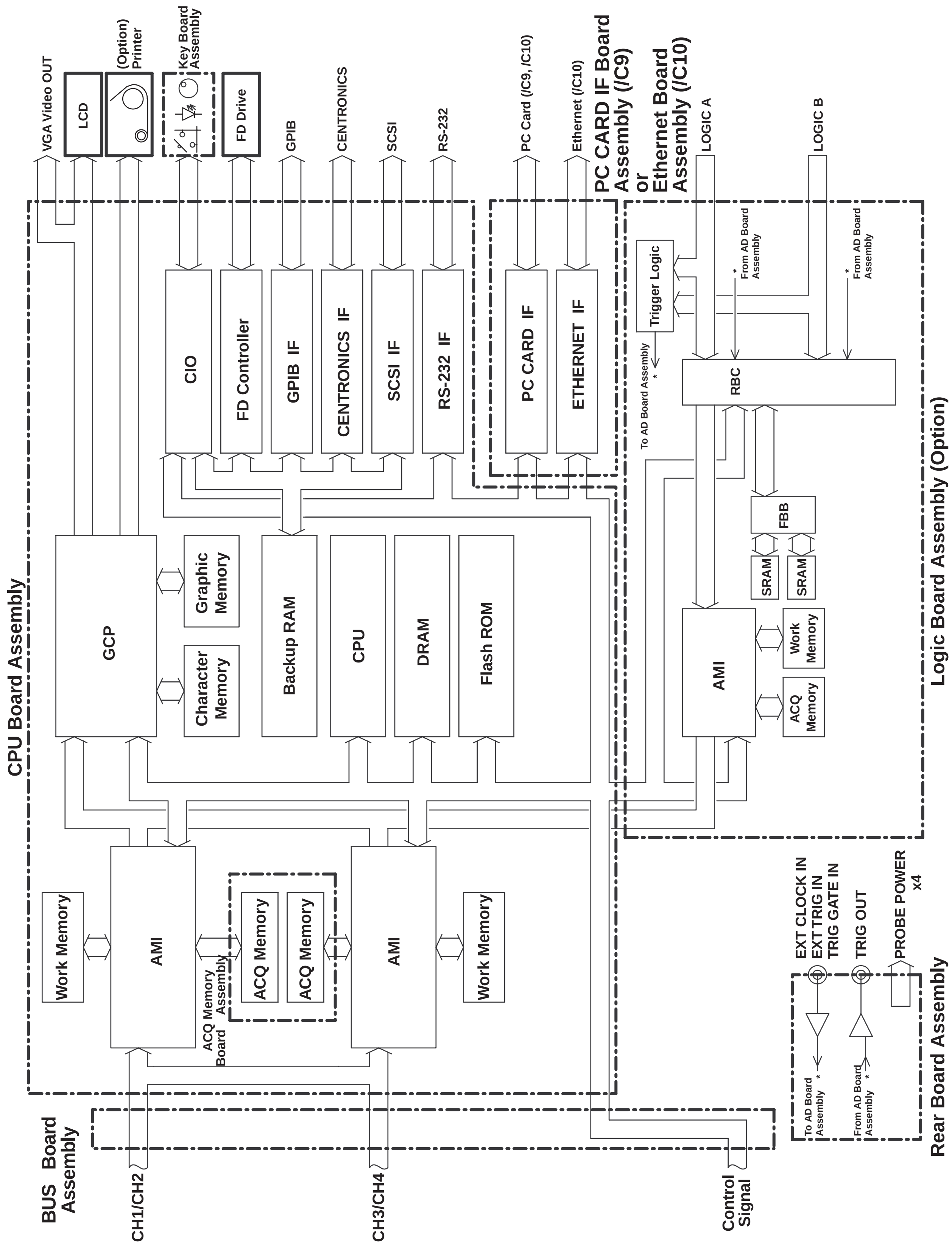


Figure 4.2 Block Diagram (Digital Section) of the DL7100

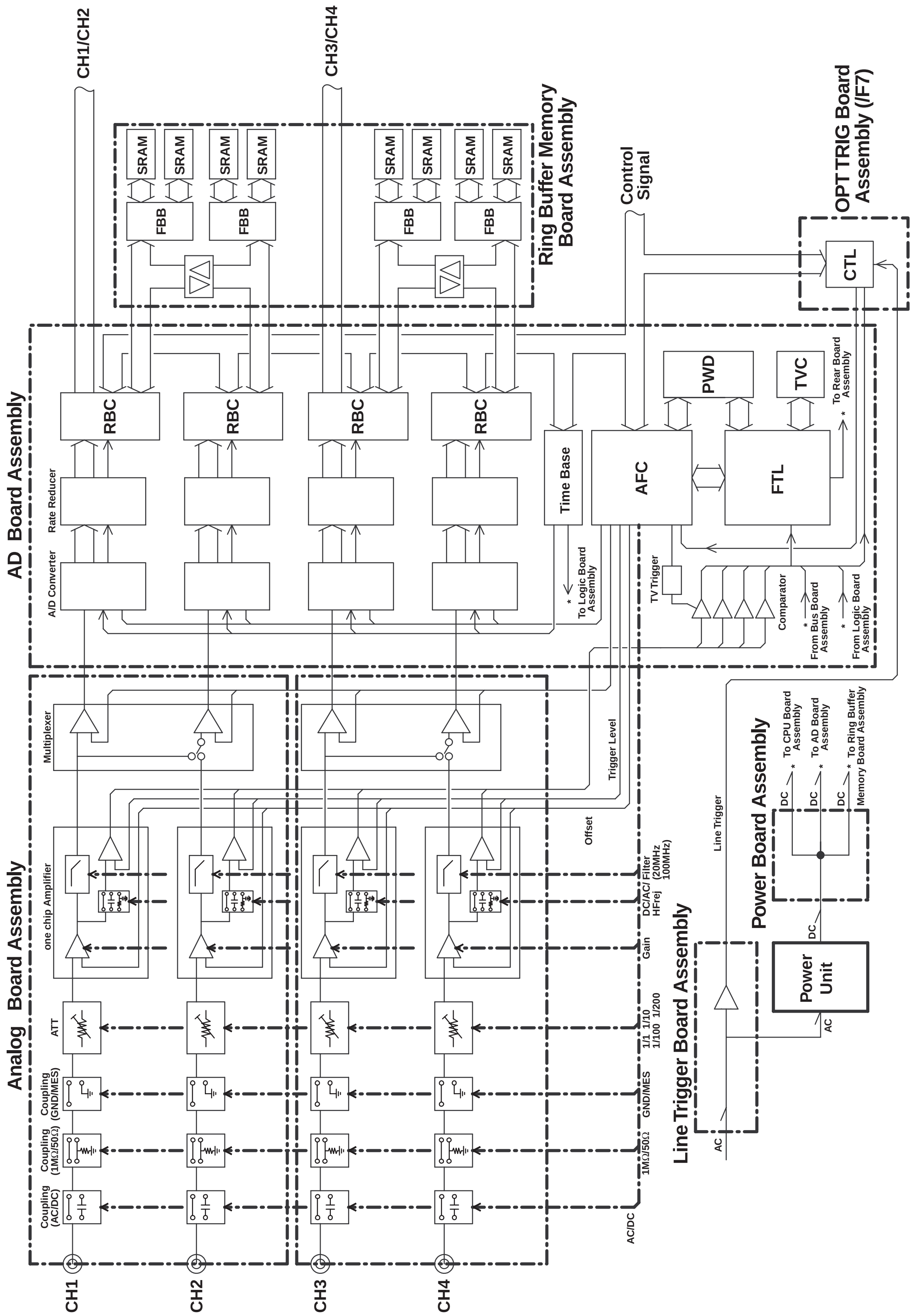


Figure 4.3 Block Diagram (Analog Section) of the DL7200

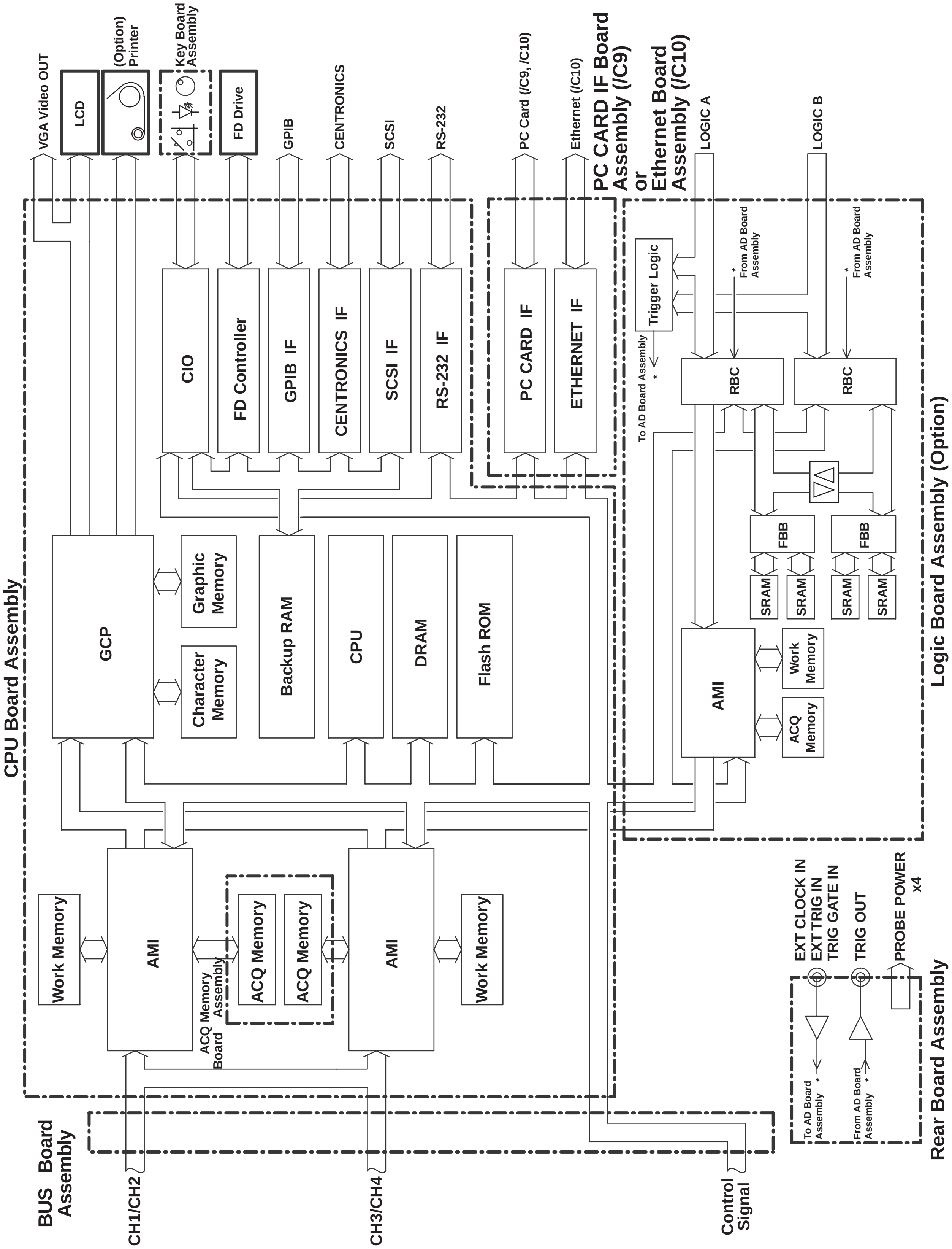


Figure 4.4 Block Diagram (Digital Section) of the DL7200

Chapter 5 TROUBLESHOOTING

Contents of This Chapter

5.1 Introduction

This chapter describes possible solutions for rectifying errors.
In such cases, assembly removal may be required.
Please keep the following precautions in mind.

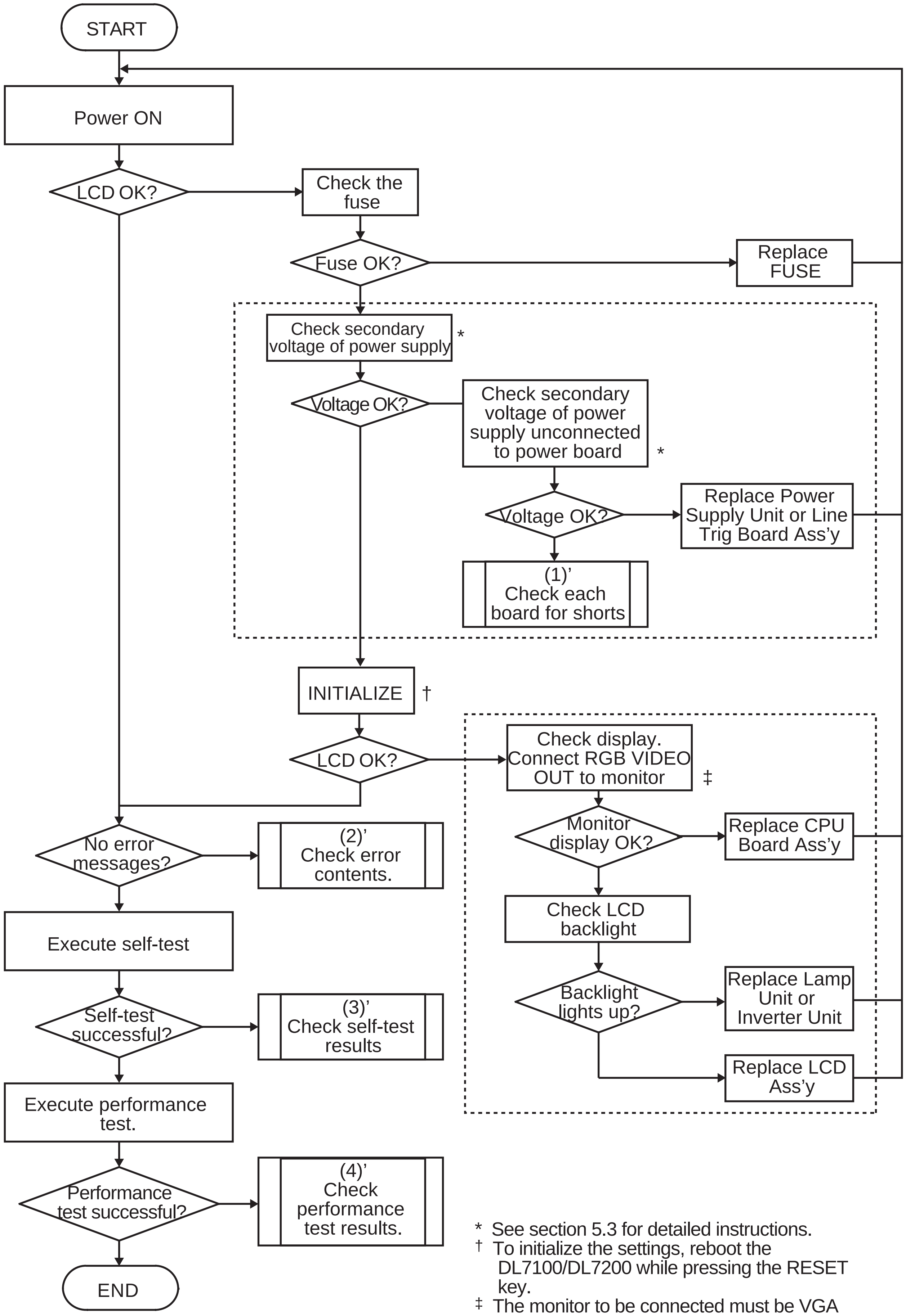
WARNING Assembly replacement is to be performed only by qualified service technicians who have experience working with the hazards involved (such as fire and electrical shock).

NOTE If an error message is displayed, the error may have been caused by incorrectly operating the unit. Refer to the user's manual, and perform the correct operation.

5.2 Flowchart

Figure 5.1, "Troubleshooting Flowchart" shows an analytical method for handling malfunctions.

(1)



* See section 5.3 for detailed instructions.
† To initialize the settings, reboot the DL7100/DL7200 while pressing the RESET key.
‡ The monitor to be connected must be VGA

Maintenance Service is Required
Contact your nearest YOKOGAWA representative as listed on the back cover of this manual.

Figure 5.1 Troubleshooting Flowchart

(1)’

A short may occur in an assembly other than the power supply unit.
To check in which voltage line a short has occurred, investigate each assembly to which voltage is supplied, using a circuit tester.
Table 5.1, “Correspondence of Assembly to Voltage” shows the relationship between assemblies and voltages supplied to them.

Table 5.1 Correspondence of Assembly to Voltage

Voltage Series	Assembly No.	Assembly
+3.3V	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
	B9969MC	CPU Board Assembly
	B9969MD	RB MEM2M Board Assembly (Model: 701410)
	B9969ME	RB MEM8M Board Assembly (Model: 701420)
	B9986MD	RB MEM4M Board Assembly (Model: 701430)
	B9986ME	RB MEM16M Board Assembly (Model: 701440)
	B9969MF	ACQ MEM Board Assembly (Model: 701410, 701420)
	B9986MF	ACQ MEM Board Assembly (Model: 701430, 701440)
	B9969MH	LOGIC2M Board Assembly (Option: /N1)
	B9969MJ	LOGIC8M Board Assembly (Option: /N2)
	B9986MH	LOGIC4M Board Assembly (Option: /N3)
	B9986MJ	LOGIC16M Board Assembly (Option: /N4)
	B9969MN	PC Card I/F Board Assembly (Option: /C9)
	B9986MG	OPT TRIG Board Assembly (Option: /F7)
	B9969MP	POWER Board Assembly
	B9969MQ	LCD Board Assembly
	B9969MT	PC Card I/F + Ethernet Board Assembly (Option: /C10)
	A1057VA	LCD Unit
+5.0V	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
	B9969MC	CPU Board Assembly
	B9969MH	LOGIC2M Board Assembly (Option: /N1)
	B9969MJ	LOGIC8M Board Assembly (Option: /N2)
	B9986MH	LOGIC4M Board Assembly (Option: /N3)
	B9986MJ	LOGIC16M Board Assembly (Option: /N4)
	B9969MK	KEY Board Assembly
	B9969ML	LINE TRG Board Assembly
	B9969MN	PC Card I/F Board Assembly (Option: /C9)
	B9986MG	OPT TRIG Board Assembly (Option: /F7)
	B9969MP	POWER Board Assembly
	B9969MR	REAR Board Assembly
	B9969MT	PC Card I/F + Ethernet Board Assembly (Option: /C10)
	B9969EA	PRINTER Assembly (Option: /B5)
	A1092UN	FDD Unit
-5.2V	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
	B9969MC	CPU Board Assembly
	B9969MH	LOGIC2M Board Assembly (Option: /N1)
	B9969MJ	LOGIC8M Board Assembly (Option: /N2)
	B9986MH	LOGIC4M Board Assembly (Option: /N3)
	B9986MJ	LOGIC16M Board Assembly (Option: /N4)
	B9969MP	POWER Board Assembly
	B9969MR	REAR Board Assembly
+12V	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
	B9969MC	CPU Board Assembly
	B9969MP	POWER Board Assembly
	B9969MR	REAR Board Assembly
	A1476UP	INVERTER Unit
-12V	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
	B9969MH	LOGIC2M Board Assembly (Option: /N1)
	B9969MJ	LOGIC8M Board Assembly (Option: /N2)
	B9986MH	LOGIC4M Board Assembly (Option: /N3)
	B9986MJ	LOGIC16M Board Assembly (Option: /N4)
	B9969MR	REAR Board Assembly
+24V	B9969MC	CPU Board Assembly
	B9969EA	PRINTER Assembly (Option: /B5)
	B9969SA	FAN Assembly

* The assembly number differs depending on the date of manufacture as follows:
During or before June, 2001: B9969MA
July, 2001 — December, 2001: B9989MA
After December, 2001: B9989ML

(2)

When trouble occurs, refer to the instruction manual to determine whether the trouble was caused by erroneous operation or by a hardware defect. Table 5.2, "Correspondence of Messages to Defective Assemblies," shows which a trouble may be due to a hardware failure.

Table 5.2 Correspondence of Massages to Defective Assemblies

Code	Message	Assembly No.	Assembly
713	Calibration failure. •••	B9989ML*	ANALOG Board Assembly
		B9969MB	AD Board Assembly (Model: 701410, 701420)
		B9986MB	AD Board Assembly (Model: 701430, 701440)
		B9969MC	CPU Board Assembly
		B9969MD	RB MEM2M Board Assembly (Model: 701410)
		B9969ME	RB MEM8M Board Assembly (Model: 701420)
		B9986MD	RB MEM4M Board Assembly (Model: 701430)
		B9986ME	RB MEM16M Board Assembly (Model: 701440)
		B9969MF	ACQ MEM Board Assembly (Model: 701410, 701420)
		B9986MF	ACQ MEM Board Assembly (Model: 701430, 701440)
		B9969MM	BUS Board Assembly
901	Failed to backup setup data. •••	B9969MC	CPU Board Assembly
906	Fan stopped •••	B9969SA	FAN Assembly
907	Backup battery is flat.	B9969MC	CPU Board Assembly

* The assembly number differs depending on the date of manufacture as follows:
During or before June, 2001: B9969MA
July, 2001 — December, 2001: B9989MA
After December, 2001: B9989ML

(3)

When trouble occurs, check the test item displaying FAIL and select the relevant defective item from table 5.3, "Correspondence of Test Items to Defective Assemblies." If necessary, replace the relevant assembly.

Table 5.3 Correspondence of Test Item to Defective Assemblies

Test item	Assembly No.	Assembly
Key Board	B9969MC	CPU Board Assembly
	B9969MK	KEY Board Assembly
Memory	B9969MC	CPU Board Assembly
FDD	B9969MC	CPU Board Assembly
	A1092UN	FDD Unit
SCSI	B9969MC	CPU Board Assembly
Printer	B9969MC	CPU Board Assembly
	B9969EA	PRINTER Assembly (Option: /B5)
Accuracy	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
	B9969MC	CPU Board Assembly
	B9969MD	RB MEM2M Board Assembly (Model: 701410)
	B9969ME	RB MEM8M Board Assembly (Model: 701420)
	B9986MD	RB MEM4M Board Assembly (Model: 701430)
	B9986ME	RB MEM16M Board Assembly (Model: 701440)
	B9969MF	ACQ MEM Board Assembly (Model: 701410, 701420)
	B9986MF	ACQ MEM Board Assembly (Model: 701430, 701440)
	B9969MM	BUS Board Assembly
PC Card	B9969MC	CPU Board Assembly
	B9969MN	PC Card I/F Board Assembly (Option: /C9)
	B9969MT	PC Card I/F + Ethernet Board Assembly (Option: /C10)

* The assembly number differs depending on the date of manufacture as follows:
During or before June, 2001: B9969MA
July, 2001 — December, 2001: B9989MA
After December, 2001: B9989ML

(4)

When trouble occurs, check the non-conforming test and select the relevant defective assembly from table 5.4, "Correspondence of Test Items to Defective Assemblies." If necessary, replace the relevant assembly.

Table 5.4 Correspondence of Test Item to Defective Assemblies

Test item	Assembly No.	Assembly
2.5 Vertical Axis DC Voltage Accuracy Test	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
2.6 Frequency Response Test	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
2.7 Time-base Accuracy Test	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
2.8 Trigger Sensitivity Test	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
2.9 Trigger Accutracy Test	B9989ML*	ANALOG Board Assembly
	B9969MB	AD Board Assembly (Model: 701410, 701420)
	B9986MB	AD Board Assembly (Model: 701430, 701440)
2.10 Logic Input Function Test	B9969MH	LOGIC2M Board Assembly (Option: /N1)
	B9969MJ	LOGIC8M Board Assembly (Option: /N2)
	B9986MH	LOGIC4M Board Assembly (Option: /N3)
	B9986MJ	LOGIC16M Board Assembly (Option: /N4)

* The assembly number differs depending on the date of manufacture as follows:
During or before June, 2001: B9969MA
July, 2001 — December, 2001: B9989MA
After December, 2001: B9989ML

5.3 Power Supply Secondary Voltage

Check power supply secondary voltage if they fit the values listed on figure 5.2, "Power Supply Secondary Terminals" and Table 5.5, "Power Supply Secondary Terminal's Voltage."

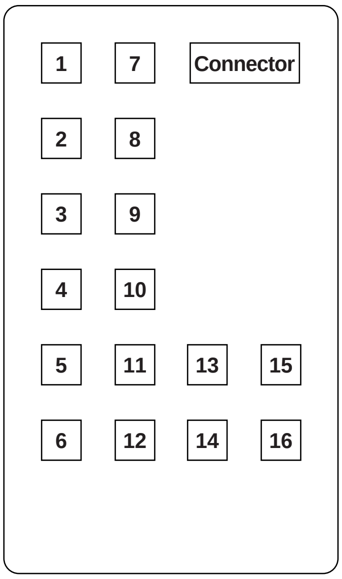


Figure 5.2 Power Supply Secondary Terminal

Table 5.5 Power Supply Secondary Terminal's Voltage

Module	Terminal	Voltage	Cable color
–5.3 V	1, 2	GND	Black
	7, 8	–5.3 V	Brown
+3.4 V*	3, 4	+3.4 V	Red
	9, 10	GND	Black
+24 V	5	+12.1 V	White
	11	GND	Black
+12.1 V	6	+5.1 V	Yellow
	12	GND	Black
+5.1 V	13	+5.1 V	Orange
	15	GND	Black
–12.1 V	14	GND	Black
	16	–12.1 V	Blue

* +3.58 V for Models 701430 and 701440.

To release the security function while checking voltage without connecting the power supply secondary terminal to the power board, short pins number 1 and 4 (See figure 5.3, "Release Security Function") of the connector shown in figure 5.2, "Power Supply Secondary Terminal." Check the voltage between terminals and GNDs of individual modules as the GNDs within each module are isolated from each other.

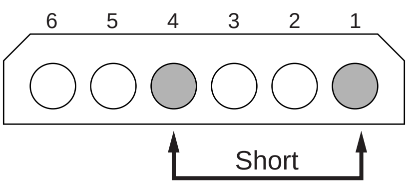


Figure 5.3 Release Security Function

5.4 Self Test

After turning the power ON, first press the **MISC** key and then the **Next 1/2** soft key. Press the **Self Test** soft key and then the **Test Item** soft key to display the **Self Test** menu screen (figure 5.4).

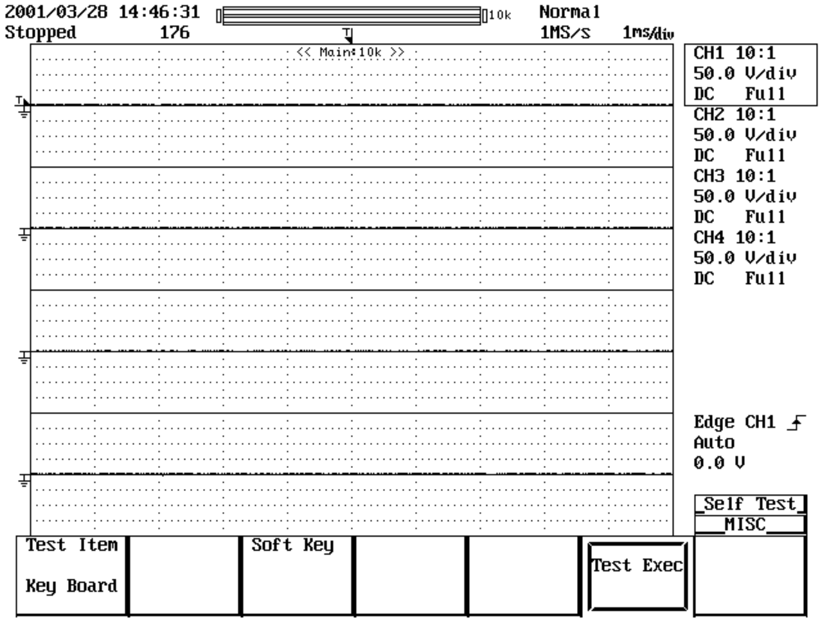


Figure 5.4 Self Test Menu

Press the soft key of the desired self-test object.

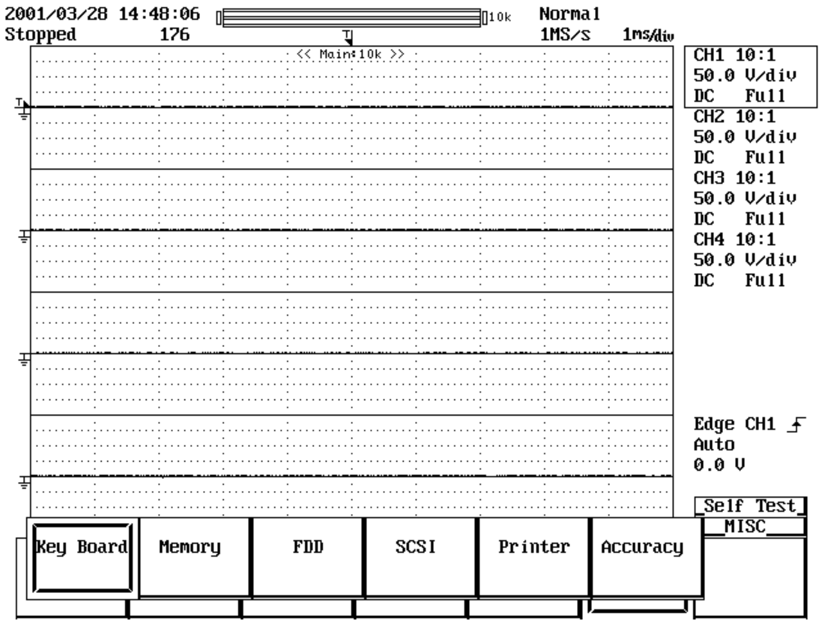


Figure 5.5 Self Test Item

5.4.1 Key Board Test

Check the operations key-switches, rotary knobs and jog-shuttle on the front panel.

1) Press the **Test Item** soft key in the **Self test** menu, and select **Key Board**. Press the **Exec** soft key to start the key test.
2) The names of each key you press should be inversely displayed on a white background. To complete the key test, press all the keys at the front panel one by one. To abort the key test, press the **ESC** key twice.

5.4.2 Memory Test

The memory test is performed and its result is displayed. When the test has been completed normally, “Pass” is displayed on the screen (refer to figure 5.6). When the test detects a problem, “Failed” is displayed on the screen. Refer to table 5.3 to select the relevant defective assembly.

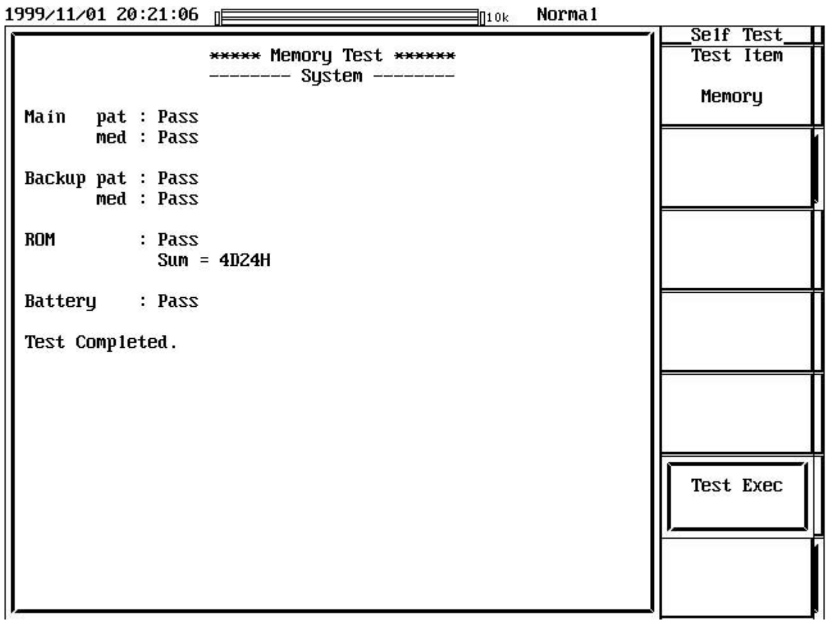


Figure 5.6 Execution Results of the Memory Test

5.4.3 FDD Test

The FDD test is performed and its result is displayed. Insert a floppy disk into the drive before executing the test. If the test has been completed normally, “Pass” is displayed on the screen (refer to figure 5.7). When the test detects a problem, “Failed” is displayed on the screen. Refer to table 5.3 to select the relevant defective assembly.

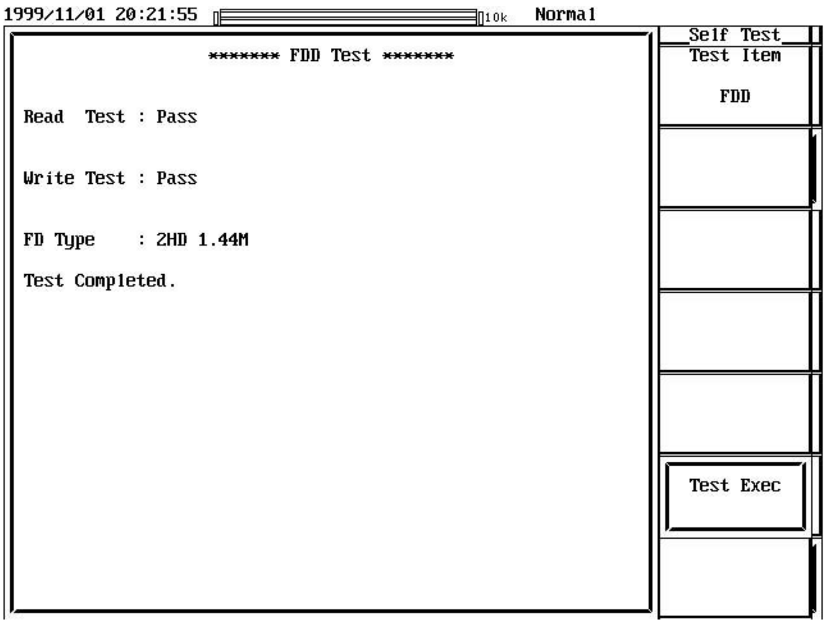


Figure 5.7 Execution Results of the FDD Test

5.4.4 SCSI Test

The SCSI test is performed and its result is displayed. When the test has been completed normally, “Pass” is displayed on the screen (refer to figure 5.8). When the test detects a problem, “Failed” is displayed on the screen. Refer to the table 5.3 to select the relevant defective assembly.

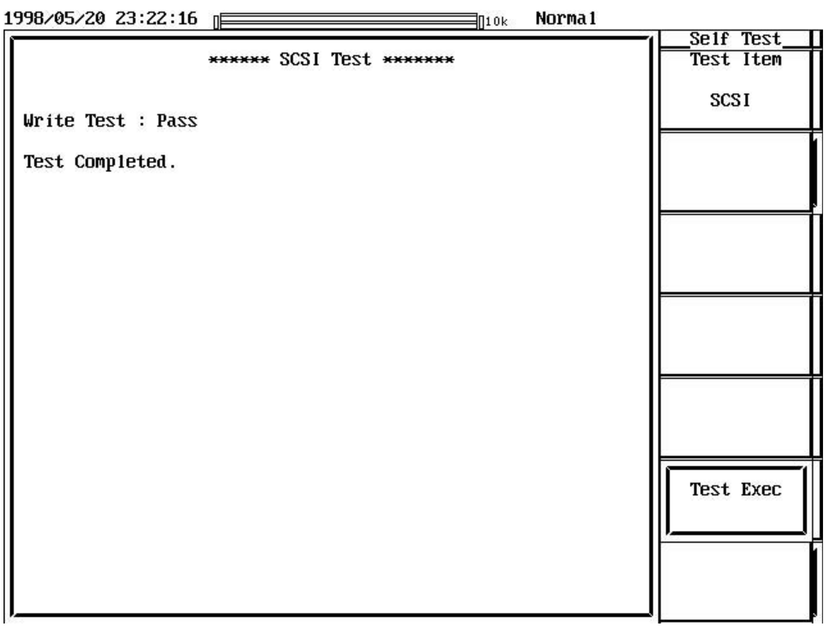


Figure 5.8 Execution Results of the Accuracy Test

5.4.5 Printer Test

If the DL7100/DL7200 is equipped with the optional printer (/B5), print out the patterns shown in figure 5.9, "Printer Print Patterns" on the printing paper.

1: Vertically printed lines on alternate dots
2: Checkered pattern every other 1 dot
3: Checkered pattern every other 2 dots
4: Checkered pattern every other 4 dots
5: Checkered pattern every other 8 dots
6: Checkered pattern every other 16 dots
7: Checkered pattern every other 32 dots
8: Checkered pattern every other 64 dots
9: Horizontally printed lines on alternate line

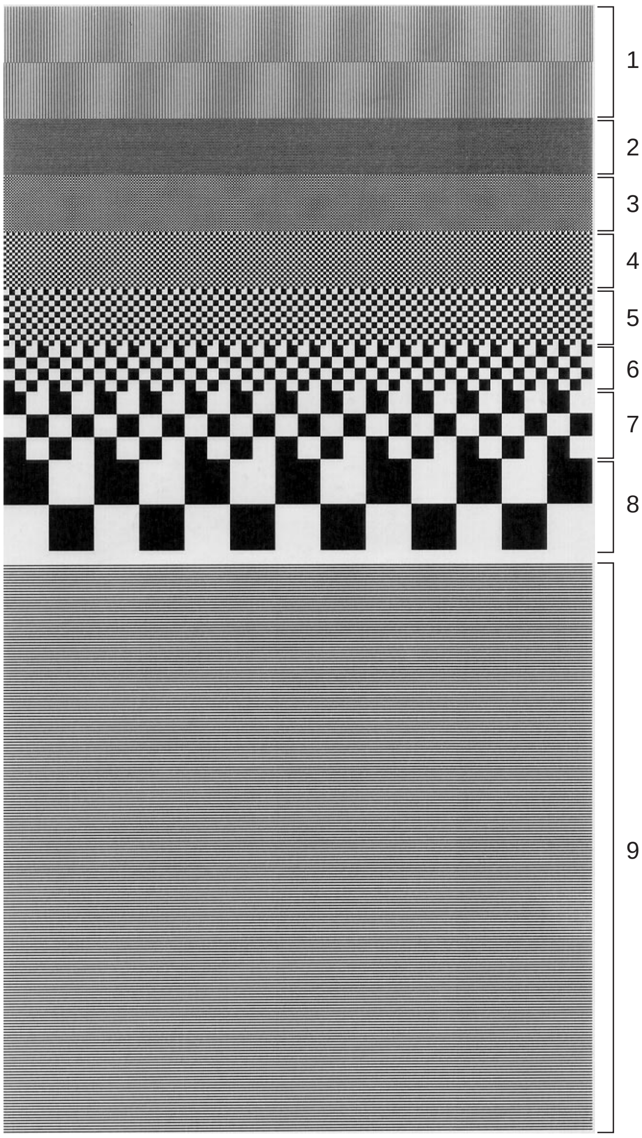


Figure 5.9 Printer Print Patterns

5.4.6 Accuracy Test

The accuracy test is performed and its result is displayed. When the test has been completed normally, "Pass" is displayed on the screen (refer to figure 5.10). When the test detects a problem, "Failed" is displayed on the screen. Refer to the table 5.3 to select the relevant defective assembly.

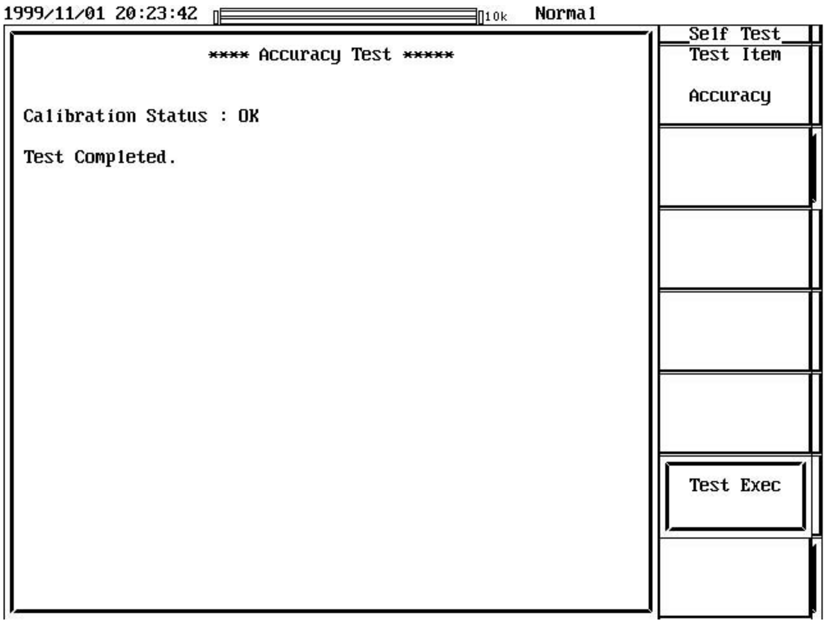


Figure 5.10 Execution Results of the Accuracy Test

5.4.7 PC Card Test (Option)

The PC card test is performed and its result is displayed. Insert a flash ATA card into the slot before executing the test. The test has been completed normally, "Pass" is displayed on the screen (refer to figure 5.11). When the test detects a problem, "Failed" is displayed on the screen. Refer to table 5.3 to select the relevant defective assembly.

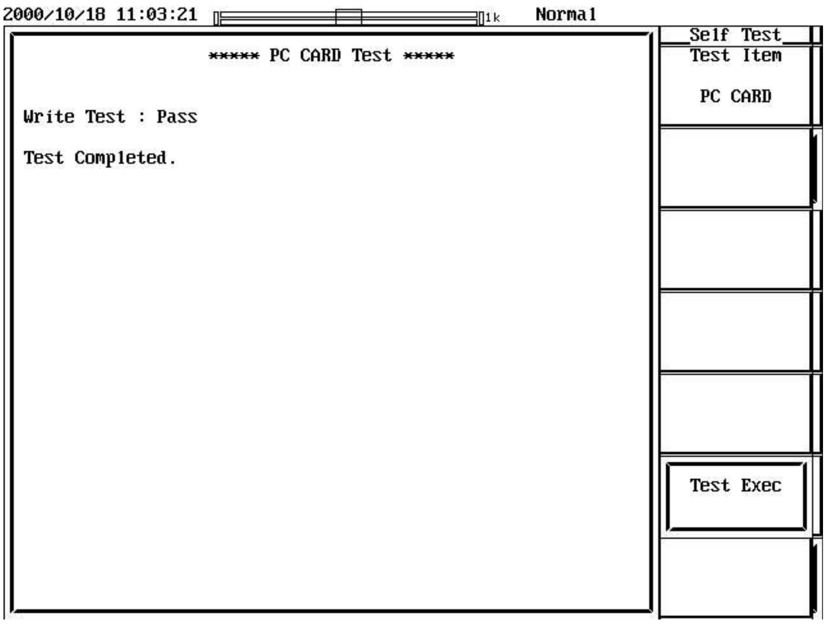
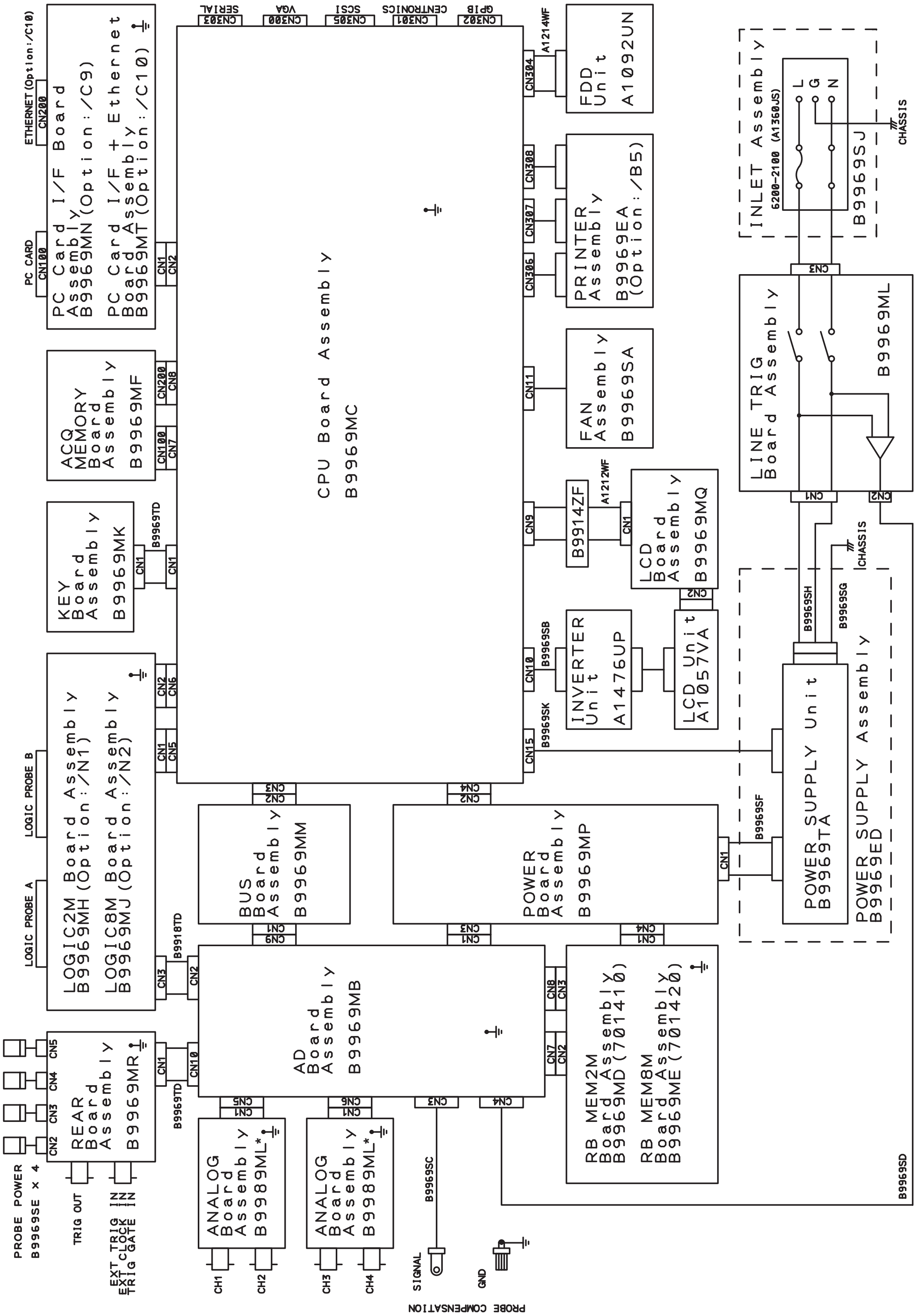


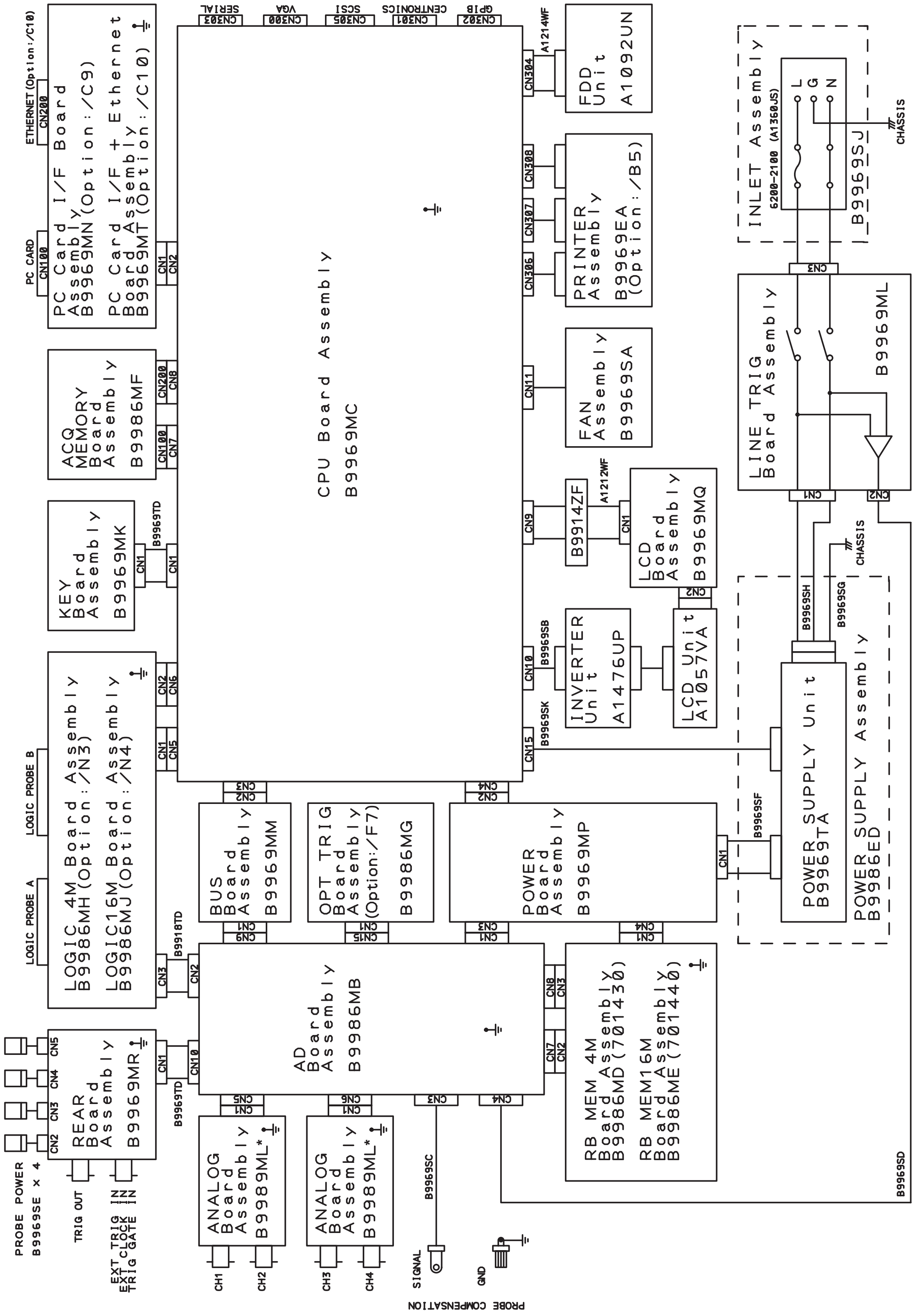
Figure 5.11 Execution Results of the PC Card Test

Chapter 6 SCHEMATIC DIAGRAM



* The assembly number differs depending on the date of manufacture as follows:
During or before June, 2001: B9969MA
July, 2001 — December, 2001: B9989MA
After December, 2001: B9989ML

Figure 6.1 Schematic Diagram of the DL7100

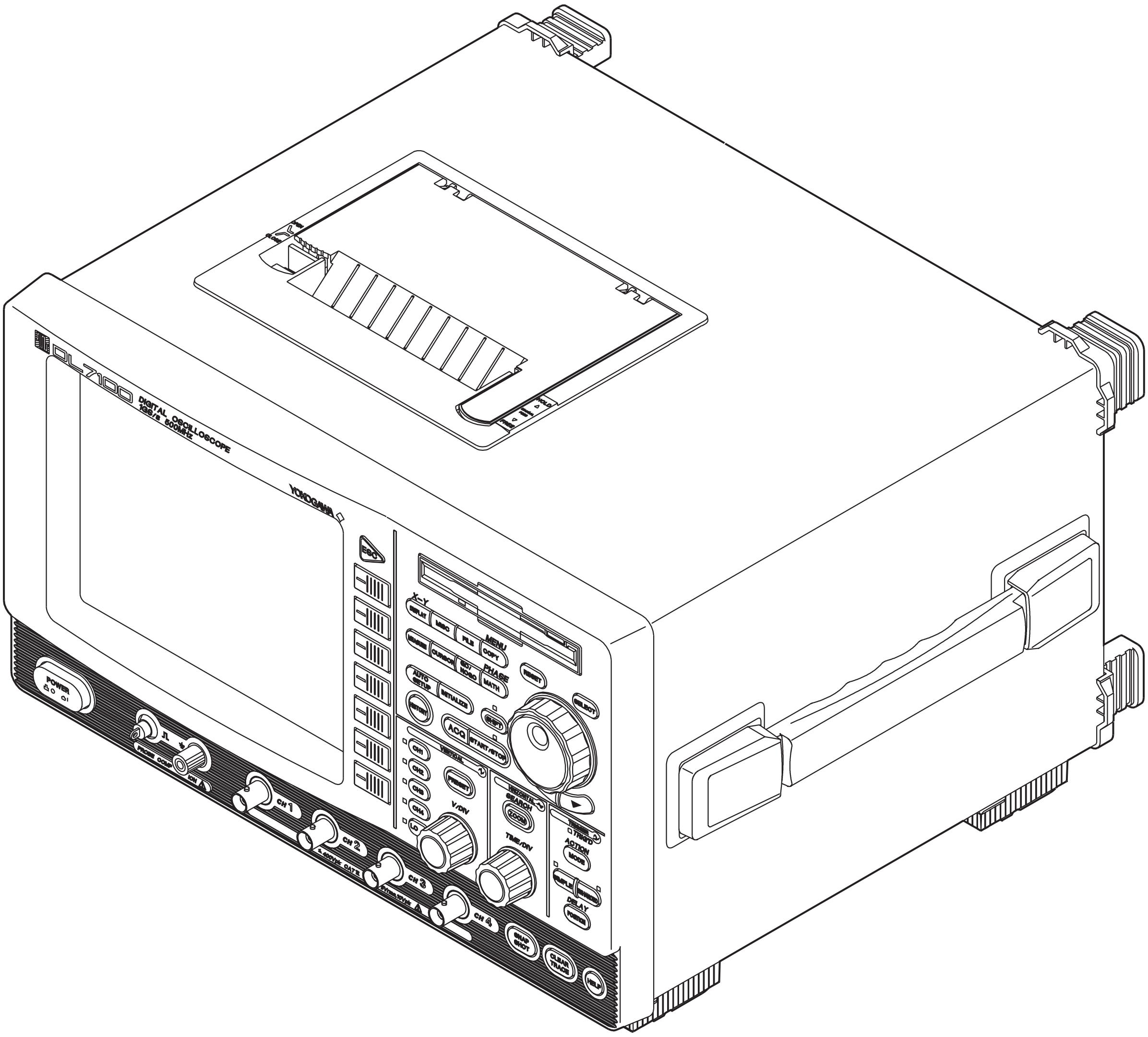


* The assembly number differs depending on the date of manufacture as follows:
During or before June, 2001: B9969MA
July, 2001 — December, 2001: B9989MA
After December, 2001: B9989ML

Figure 6.2 Schematic Diagram of the DL7200

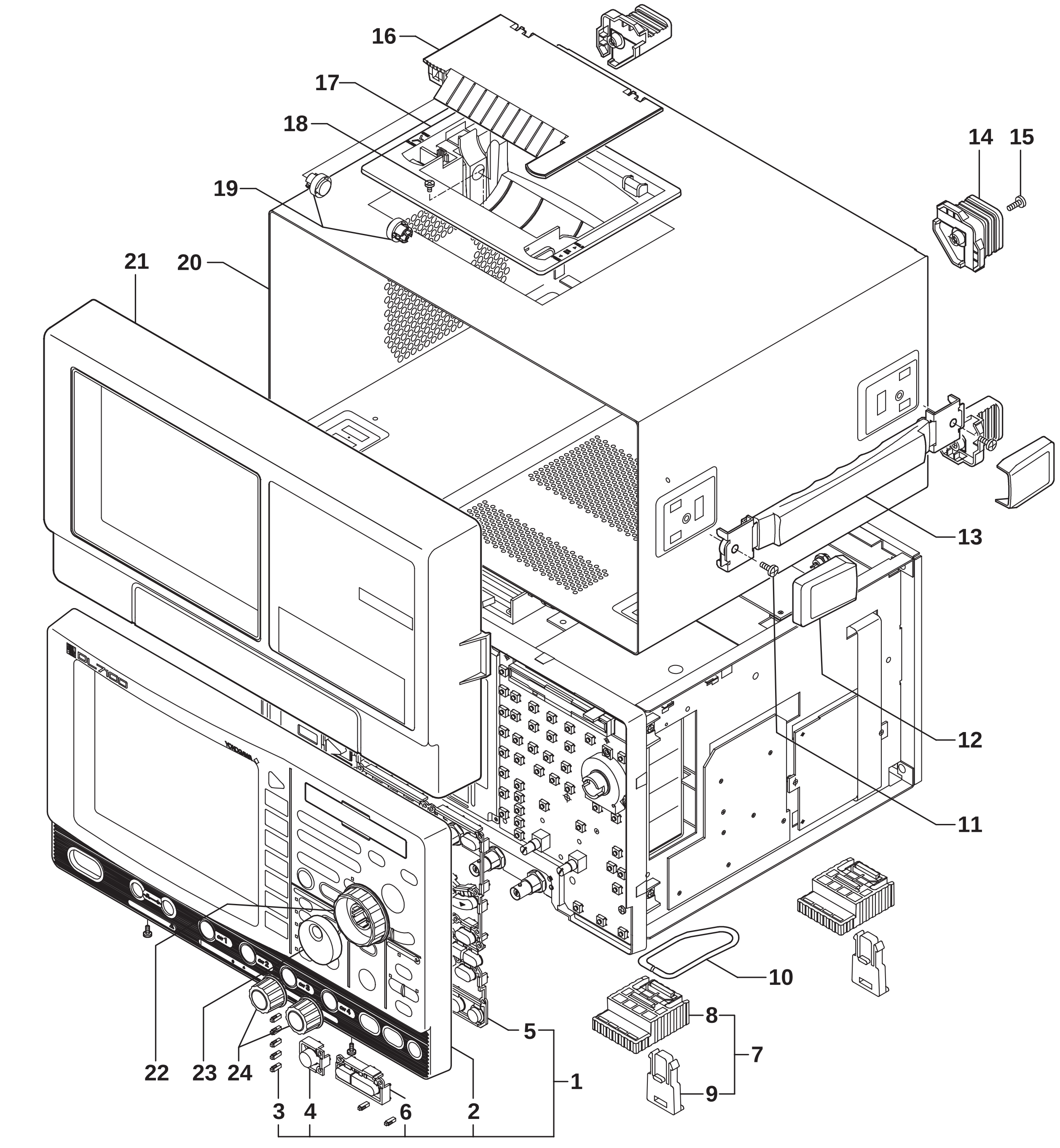
Chapter 7 CUSTOMER MAINTENANCE PARTS LIST

7.1 Customer Maintenance Parts List



Note:

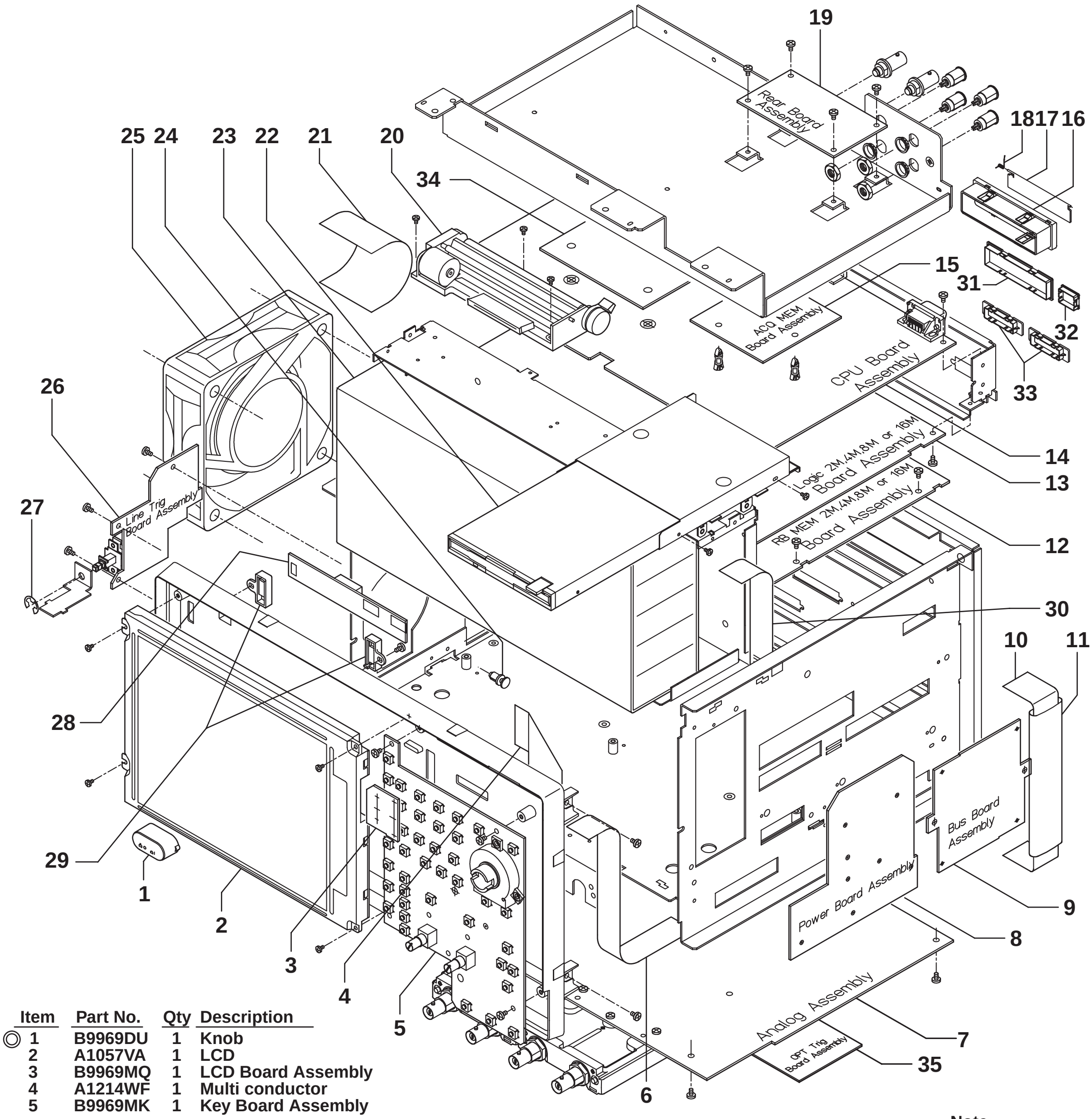
Parts marked with a ◎ symbol are CMPL (Customer maintenance parts list) parts.



Item	Part No.	Qty	Description	
1	B9969DA	1	Front Bezel Assembly (701410, 701420)	(select)
	B9986DA	1	Front Bezel Assembly (701430 not /F7, 701440 not /F7)	
	B9986EH	1	Front Bezel Assembly (701430 /F7, 701440 /F7)	
2	B9969DB	1	Front Bezel (701410, 701420)	(select)
	B9986DB	1	Front Bezel (701430, 701440)	
	B9986DE	1	Front Bezel (701430 /F7, 701440 /F7)	
3	B9969DK	10	Lens	
4	B9969DD	1	Knob	
5	B9969DC	1	Knob	
6	B9969DE	1	Knob	
◎ 7	A9120ZM	4	Foot Assembly	
8	A9083ZM	1	Foot	
9	A9110ZM	1	Spacer	
◎ 10	A9086ZM	2	Support	
◎ 11	Y9512LB	2	Screw	

Item	Part No.	Qty	Description	
◎ 12	A9065ZM	2	Cover	
◎ 13	B9969EQ	1	Grip Assembly	
◎ 14	B9969DV	4	Rear Foot	
◎ 15	Y9418LB	4	B.H. Screw, M4x18	
◎ 16	A9137ZM	1	Cover (/B5)	
17	A9136ZM	1	Case (/B5)	
18	B9946GZ	2	Screw (/B5)	
◎ 19	A9079ZM	2	Knob (/B5)	
20	B9969CX	1	Case Assembly (701410, 701420 /B5)	(select)
	B9969DX	1	Case Assembly (701410, 701420 not /B5)	
	B9986CX	1	Case Assembly (701430, 701440 /B5)	
	B9986DX	1	Case Assembly (701430, 701440 not /B5)	
◎ 21	B9969BY	1	Front Cover (see page 7-4)	
◎ 22	B9969DG	1	Knob	
◎ 23	B9969DH	1	Knob	
◎ 24	B9969DJ	2	Knob	

Note :
◎ CMPL parts



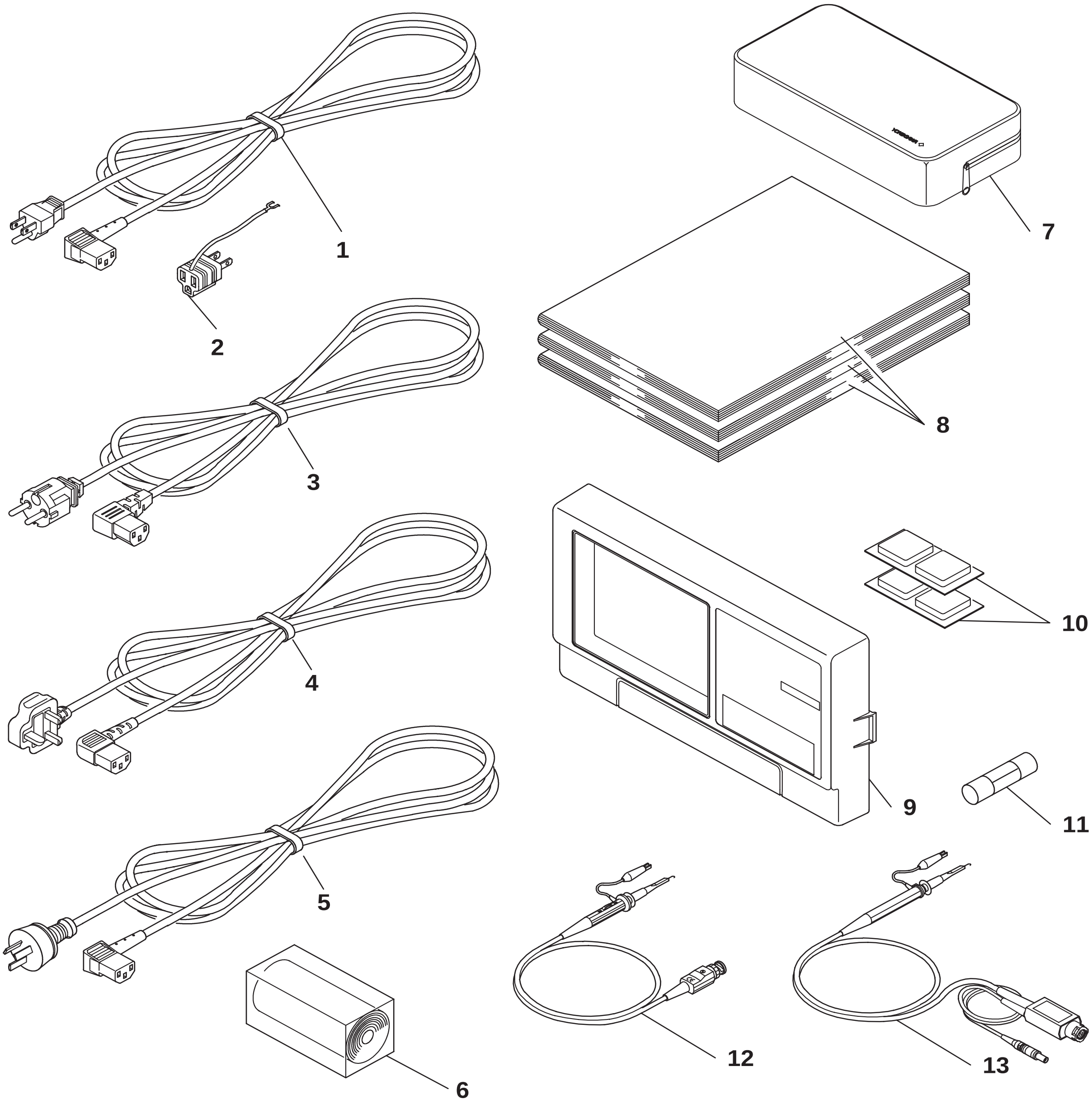
Item	Part No.	Qty	Description	
◎ 1	B9969DU	1	Knob	
2	A1057VA	1	LCD	
3	B9969MQ	1	LCD Board Assembly	
4	A1214WF	1	Multi conductor	
5	B9969MK	1	Key Board Assembly	
6	B9969TD	1	Cable	
7	B9969EC	1	Analog Board Assembly (701410, 701420)	(select)
	B9986EC	1	Analog Board Assembly (701430, 701440)	
8	B9969MP	1	Power Board Assembly	
9	B9969MM	1	Bus Board Assembly	
10	B9969TD	1	Cable	
11	A9425XK	1	Tube	
12	B9969MD	1	RB MEM 2M Board Assembly (701410)	(select)
	B9969ME	1	RB MEM 8M Board Assembly (701420)	
	B9986MD	1	RB MEM 4M Board Assembly (701430)	
	B9986ME	1	RB MEM 16M Board Assembly (701440)	
13	B9969MH	1	Logic 2M Board Assembly (/N1)	(select)
	B9969MJ	1	Logic 8M Board Assembly (/N2)	
	B9986MH	1	Logic 4M Board Assembly (/N3)	
	B9986MJ	1	Logic 16M Board Assembly (/N4)	
14	B9969MC	1	CPU Board Assembly	
15	B9969MF	1	ACQ MEM Board Assembly (701410, 701420)	
	B9986MF	1	ACQ MEM Board Assembly (701430, 701440)	
16	B9969DQ	1	PC Card Bezel (/C9) (/C10)	
17	B9969DR	1	PC Card Cover (/C9) (/C10)	

Note :

◎ CMPL parts

Item	Part No.	Qty	Description	
18	B9969DS	1	Spring (/C9) (/C10)	
19	B9969MR	1	Rear Board Assembly	
20	A1207UD	1	Printer (/B5)	
21	B9918TD	1	Cable (/N1, /N2, /N3, /N4)	
22	A1092UN	1	Memory System	
23	B9969ED	1	Power Supply Assembly (701410, 701420)	(select)
	B9986ED	1	Power Supply Assembly (701430, 701440)	
24	B9969BX	4	Rivet	
25	B9969SA	1	Fan Assembly	
26	B9969ML	1	Line Trig Board Assembly	
27	Y9250ET	1	Retainer E	
28	A1476UP	1	Power Supply	
29	B9946DG	2	Spacer	
30	A1214WF	1	Multi conductor	
◎ 31	B9986DC	1	Cover (not /C10, /C9)	
◎ 32	B9986DD	1	Cover (not /C10)	
◎ 33	A9066ZB	2	Cap (not /N1, /N2, /N3, /N4)	
34	B9969EB	1	PC Card Assembly (/C9)	(select)
	B9969FC	1	PC Ether Assembly (/C10)	
35	B9986MG	1	OPT TRIG Board Assembly (701430 /F7, 701440 /F7)	

7.2 Standard Accessories



	Item	Part No.	Qty	Description	
◎	1	A1006WD	1	Power Supply Code (UL/CSA standard) *, †	(select)
◎	2	A1253JZ	1	3P-2P Adapter *	(select)
◎	3	A1009WD	1	Power Supply Code (VDE standard) ‡	(select)
◎	4	A1054WD	1	Power Supply Code (BS standard) §	(select)
◎	5	A1024WD	1	Power Supply Code (AS standard) ‖	(select)
◎	6	B9850NX	1	Roll Chart (/B5)	
◎	7	B9969ET	1	Soft Case	
	8	IM701410-01E	1	DL7100/DL7200 Digital Oscilloscope User's Manual	
		IM701410-02E	1	DL7100/DL7200 Digital Oscilloscope Operation Guide	
		IM701410-01E	1	DL7100/DL7200 Digital Oscilloscope Communication Interface	
		IM701410-01E	1	DL7200 CAN Bus Signal Analysis Function #	
◎	9	B9969BY	1	Front Cover	
◎	10	A9088ZM	2	Stopper	
◎	11	A1352EF	2	Fuse	
◎	12	700988	2	Probe	
		700988	2	Probe (/E2)	
◎	13	700939	2	FET Probe (/E3)	

Note:

*	7014☐☐-☐-M
†	7014☐☐-☐-D
‡	7014☐☐-☐-F
§	7014☐☐-☐-Q
‖	7014☐☐-☐-R
#	701430, 701440
◎	CMPL parts